PUNE VIDYARTHI GRIHA'S

COLLEGE OF SCIENCE AND TECHNOLOGY

Affiliated to University of Mumbai

Question Bank

Class: S.Y.B. Sc.IT **Semester: IV**

Subject: Introduction to Embedded Systems

Question	A	B	C	D
What is CISC?	Computing instruction set complex	Complex instruction set computing	Complementary instruction set computing	Complex instruction set complementary
RISC allows _____	Orthogonal Instruction set	Non-orthogonal Instruction set	Greater number of instructions	No instruction pipelining
A technique that allows for simultaneous execution of parts, or stages, of instructions to more efficiently process instructions is called as	Embedded system	instruction pipelining	Orthogonal Instruction set	Non-orthogonal Instruction set
What kind of visual panel is used for seven segmented display?	LED	DAC	Binary output	Analogue output
An embedded system is a combination of ----------	hardware, software, memory	hardware, firmware, mechanical component	hardware, system bus, memory	Cpu, i/o and memory
An embedded system can do _____ task	multi task at a time	single task at a time	specific task	sometime multitask sometime single task
Embedded systems are ----------	general purpose	special purpose	domain purpose	general and special purpose
An embedded system must have	hard disk	processor and memory	operating system	processor and input-output unit
Which of the following is not an example of a 'Small scale embedded System'?	Electronic Barbie doll	simple calculator	Cell phone	Electronic toy car
Which of the following is not intended purpose(s) of embedded systems?	Data Collection	Data Processing	Data Communication	Data Cleaning
Which of the following is an example of embedded system for data communication?	USB Mass storage device	Network router	Digital camera	Music player

Little Endian Processor means	Store the lower order byte of the data at the lowest address and the higher order byte of the data at the highest address memory	Store the higher-order byte of the data at the lowest address and the lower order-byte of the data at the highest address of memory	Store both higher order and lower order byte of the data at the same address of memory	Store both higher order and lower byte of the data at the higher address of memory
The instruction set of RISC processor is	Simple and lesser in number	complex and lesser in number	Simple and larger in number	Complex and larger in number A
Which characteristics of an embedded system exhibit the responsiveness to the assortments or variations in system's environment by computing specific results for real-time applications without any kind of postponement ?	Single-functioned Characteristic	Non-operational Characteristics	Reactive & Real time Characteristics	Operational characteristics
What is the directional nature of two active wires SDA & SCL usually adopted in I2C Bus for carrying the information between the devices ?	Uni-directional	Bi-directional	Multi-directional	Semi-directional
Which potential mode of operation indicate the frequent sending of byte to the slave corresponding to the reception of an acknowledge signal when it becomes desirable for the master to write to the slave during data transmission in I2C bus?	Master in master-transmit mode & Slave in slave-receive mode	Slave in slave-transmit mode & Master in master-receive mode	Master in master-transmit mode as well as master-receive mode	Slave in slave-transmit mode as well as slave-receive mode
Which among the below not stated salient feature of SPI contribute to the wide range of its applicability?	Simple hardware Interfacing	Full duplex communication	low power requirement	supports acknowledgement mechanism
Which development tool / program has the potential to allocate the specific addresses so as to load the object code into memory?	Loader	Locator	Library	Linker
Which architectural scheme has a provision of two sets for address & data buses between CPU and memory?	Harvard architecture	Von-Neumann architecture	Princeton architecture	Stanford architecture
Microprocessors/controllers based on the _____ architecture shares a single common bus for fetching both instructions and data	Harvard architecture	Von-Neumann architecture	Princeton architecture	Stanford architecture
Which is not operational quality attribute?	Response	Throughput	Reliability	Time to market

Which is/are the non-operational quality attribute?	Testability and Debug-ability	safety	security	reliability
_____deals with the possible damage that can happen to the operating person and environment due to the breakdown of an embedded system or due to the emission of hazardous materials from the embedded products.	Testability and Debug-ability	safety	security	reliability
Confidentiality, Integrity and Availability are three corner stones of _____	Testability and Debug-ability	safety	security	reliability
A digital multimeter is an example of an embedded system used for the purpose of	data collection	data processing	data communication	data monitoring
Throughput of an embedded system is a measure of	efficiency of the system	output over a stated period of time	input over a period of time	performance Criteria
The instruction set of RISC processor is	Simple and lesser in number	complex and lesser in number	Simple and larger in number	Complex and larger in number
Medium-scale embedded systems are usually built around medium performance, low cost _____ bit microprocessors/ micro-controllers or digital signal processors.	8 – 16	16 – 32	4 – 8	32 – 64
A _____ is a highly integrated chip that contains a CPU, scratch pad RAM, special and general purpose register arrays, in chip ROM/FLASH memory for program storage, timer and interrupt control units and dedicated I/O ports	Microprocessor	Microcontroller	DSP	ASIC
A _____ product is one which is used 'as-is'	DSP	ASIC	PLD	COTS
_____ is a device that when exposed to a physical phenomenon (temperature, displacement, force, etc.) produces a proportional output signal (electrical, mechanical, magnetic, etc.).	Actuator	Sensor	Transducer	Thermometer
Smart phone devices, mobile internet devices (MIDs), etc. are examples of _____ generation embedded systems.	First	Second	Third	Forth
_____ released in 1974, is considered as the world's first microcontroller.	Intel 8085	Intel 4004	TMS 1000	TMS 5000
_____ can be viewed as a microchip designed for	DSP	ASIC	PLD	COTS

performing high speed computational operations for ‘addition’, ‘subtraction’, ‘multiplication’ and ‘division’.				
_____ means the higher-order byte of the data is stored in memory at the lowest address and the lower-order byte at the highest address.	Little endian	Big endian	Small endian	Large endian
_____ is a kind of integrated circuit that is specially built for a specific application or purpose.	DSP	ASIC	PLD	COTS
These are custom-made from scratch for a specific application. Their ultimate purpose is decided by the designer.	Full Custom ASIC	Semi-Custom ASIC	Half Custom ASIC	Platform ASIC
_____ accepts a control command (mostly in the form of an electrical signal) and produces a change in the physical system by generating force, motion, heat, flow, etc.	Actuator	Sensor	Transducer	Thermometer
_____ low cost, low power, short range wireless technology for data and voice communication which supports point to point and multi point communication	Wifi	Bluetooth	Infrared	UART
The _____ circuit brings the internal registers and the different hardware systems of the	processor/controller to a known state and starts the firmware execution from the reset vector.	Brownout protection	Watchdog	Reset
_____ prevents the processor/controller from unexpected program execution behaviour when the supply voltage to the processor/controller falls below a specified voltage.	Brownout protection	Watchdog	Reset	Oscillator
_____is a hardware timer for monitoring the firmware execution. Depending on the internal implementation, the timer increments or decrements a free running counter with each clock pulse and generates a reset signal to reset the processor	Brownout protection	Watchdog	Reset	Oscillator
_____ is measure of quickness of the system.	Throughput	Reliability	Maintainability	Response
Mean Time Between Failures (MTBF) and Mean Time To Repair (MTTR) are the terms	Throughput	Reliability	Maintainability	Response

used in defining system's _____				
_____refers to the ease with which the embedded product can be modified to take advantage of new firmware or hardware technologies.	Portability	Maintainability	Evolvability	Reliability
Mission critical application is an example of a _____ scale embedded system.	Small	Medium	Large	Ultra large
Air conditioning system used in our home is an example of an embedded system used for the purpose of	data collection	data processing	data monitoring	data control
_____ is a dependent unit and it requires the combination of other hardware like memory, timer unit, and interrupt controller, etc. for proper functioning.	Microprocessor	Microcontroller	DSP	ASIC
Intel introduced the world's first microprocessor chip called the _____	4041	4004	8001	8085
Second generation Built around _____ microcontroller & microprocessor.	8 bit	8bit, 16bit	16bit, 32bit	32bit, 64 bit
Name a volatile memory.	RAM	EPROM	ROM	EEPROM
Which one of the following is UV erasable?	Flash memory	SRAM	EPROM	DRAM
How the input terminals are associated with external environments?	Actuators	Sensors	Inputs	Outputs
Why is SRAM more preferable in non-volatile memory?	low-cost	high-cost	low power consumption	transistor as a storage element
_____ is a ISO defined serial communication bus originally developed for the automotive industry.	CAN	LAN	WAN	MAN
_____ is the processor's address book.	memory map	IO map	Interrupt map	Polling
The _____ is the function executed called when a particular interrupt occurs.	IRS	ISR	IRR	ISS
_____ method simply uses a code section which checks a particular flag or status of operation	memory map	IO map	Interrupt map	Polling
A nonvolatile type of memory that can be programmed and erased in sectors, rather than one byte at a time is:	Flash memory	PROM	EPROM	ROM A
Memory that doesn't loses its contents when power is lost is:	Volatile memory	Non-volatile memory	RAM	Hybrid memory

What is meant by the term RAM?	Memory which can only be read	Memory which can both be read and written	Memory which is used for storing data	Memory which can only be written
The two kind of main memory are	primary and secondary	direct and sequential	floppy disk and hard disk	Primary and hybrid
Which of the following memories below is often used in typical computer operation?	SRAM	DRAM	HDD	FDD
What is the name given to the memory which works on time sharing principle in order to create an illusion of infinite memory space?	Flash memory	Virtual Memory	Cache memory	ROM B
DMA stands for _____	Direct Memory Access	Depend Memory Access	Data Memory Access	Data Memory address
_____ is a specific checksum algorithm that is designed to detect the most common data errors.	CRC	CRR	CCR	RCR
_____ is an electronic timer that is used to detect and recover from computer malfunction	Brownout protection	Watchdog	Reset	Oscillator
_____ is a method of transferring data from the computer's RAM to another part of the computer without processing it using the CPU.	DMA	DMM	AMD	DAM
There are _____ types of Hybrid memory devices	2	3	4	5
PROM is also called as _____	EPROM	OTP NVM	EEPROM	OCP NVM
Each storage location of EPROM consist of a single _____	FET	Diode	Gate	led
EDO, SD, DDR are types of _____	RAM	ROM	Flash	Cache
In response to specific event the microcontroller stops executing main code and switches to a different section called as _____	ISR	ISS	IRR	IRS
The _____ comprises of the various electronic components and circuits, which are programmed to perform in unique ways depending on the load conditions (the condition and the amount of clothes loaded in the washing machine	Motherboard	PCB	Breadboard	DSP
_____ technology in the automotive industry refers to the use of electrical or electro-mechanical systems for	Drive by wire	Lane assist	ECS	Cruise control

performing vehicle functions which were traditionally achieved by mechanical linkages/actuators				
_____ is a system that automatically controls the speed of a motor vehicle.	Drive by wire	Lane assist	ECS	Cruise control
_____ are also referred to as Supplemental Restraint System (SRS)	Drive by wire	Lane assist	Airbag control	Cruise control
In order for the processor to execute the correct ISR, a mapping must exist called as	I/O map	Interrupt map	Memory map	ISR map
_____ is a type of non-volatile RAM memory which uses magnetic charges in order to store data	RAM	SRAM	DRAM	MRAM
_____ has to be refreshed after each read operation	RAM	SRAM	DRAM	MRAM
A_____ problem could be caused by an error in design or production of the board or as the result of damage received after manufacture.	electrical wiring	Missing memory problem	Improperly inserted memory chip	Address bus
Walking 1 test is an example of	Address bus test	Data bus test	Control bus test	Device test
The width of checksum CRC32 is _____	8 bits	16 bits	32 bits	64 bits
The width of checksum GCITT is _____	8 bits	16 bits	32 bits	64 bits
The width of checksum CRC16 is _____	8 bits	16 bits	32 bits	64 bits
Initial remainder of GCITT is _____	0xFF	0x00	0xFFFF	0x0000
Initial remainder of CRC16 is _____	0xFF	0x00	0xFFFF	0x0000
_____ memory is often found in USB flash drives, MP3 players, digital cameras and solid-state drives	RAM	ROM	Flash	Cache
When _____ Flash memories are to be read, the contents must first be paged into memory-mapped RAM	NOR	NAND	OR	XOR
HECUs are deployed in critical control units requiring _____ response.	Fast	Slow	Critical	Non-critical
LECUs are built around _____ cost microprocessors and microcontrollers and digital signal processors.	Low	high	free	open
_____ embedded systems are the one where electronics take control over the mechanical system.	Retail	Healthcare	Automotive	Security

Embedded system used inside an automobile communicate with each other using _____ buses.	serial	parallel	orthogonal	non-orthogonal
_____ uses Low Speed Electronic Control Units.	fuel injection systems	antilock brake systems	engine control	Audio controller
_____ has certain features of RAM and some of ROM.	NVRAM	SRAM	EPROM	Masked ROM
A Memory Map is the processor's _____.	address book	data book	log book	interface book
In _____ technique the processor asks the device repeatedly at regular intervals to check if the device has completed the given task or has any new task to execute.	Polling	Interrupt	Interrogation	Modulation
Which of the following is an example for the input subsystem of an embedded system dealing with digital data?	ADC	DAC	Stepper Motor	LED
Which of the following is an example for the output subsystem of an embedded system dealing with digital data?	ADC	DAC	Button	Sensor
In Microwave oven, a _____ is a microwave antenna placed in a vacuum tube and oscillated in an electromagnetic field in order to produce high GHz microwaves.	Electron gun	Cavity gun	Cavity magnetron	Electron magnetron
8051 has _____ bytes of RAM.	64	128	256	512
8052 has _____ bytes of RAM.	64	128	256	512
8031 has _____ bytes of RAM.	64	128	256	512
8051 has _____ ROM.	0K	4K	8K	16K
8031 has _____ ROM.	0K	4K	8K	16K
8052 has _____ ROM.	0K	4K	8K	16K
The 8051 has _____ timers.	1	2	3	4
The 8052 has _____ timers.	1	2	3	4
The 8031 has _____ timers.	1	2	3	4
The 8031 has _____ serial port.	1	2	3	4
The I/O ports that are used as address and data for external memory are	ports 1 and 2	ports 1 and 3	ports 0 and 3	ports 0 and 2
The 8051 has _____ parallel I/O ports.	2	3	4	5
The total external data memory that can be interfaced to the 8051 is:	32K	64K	128K	256K
The 8051 has _____ I/O pins.	4	32	64	40
How many bytes of bit addressable memory is present in 8051 based micro controllers?	8 bytes	32 bytes	16 bytes	128 bytes

8052 has _____ interrupt sources.	6	8	4	2
8051 has _____ interrupt sources.	6	8	4	2
8031 has _____ interrupt sources.	6	8	4	2
8051 can execute _____ one-cycle instructions per second with a clock frequency of 12MHz	1 million	2 million	12 million	11.592 million
In 8051, Pins XTAL 1 and XTAL 2 are provide for connecting a resonant network to form an_____.	Oscillator	Register	Oscilloscope	Resistor
The crystal frequency is the basic _____ clock frequency of the microcontroller.	Peripheral	External	Internal	Solid
In 8051, the _____ register is the most versatile CPU register and is used for many operations, including addition, subtraction, integer multiplication and division.	A	B	C	D
_____is used to permanently save the program being executed.	Program Memory	Data Memory	RAM	NVRAM
For 8051, _____ datatype is most appropriate.	Int	Char	Boolean	Sbit
8051 has _____ register Bank.	2	3	4	5
Which of the following line is use to access Pin 0 of port 1.	sbit x=P1.0;	sbit x=P1^0;	sbit x=P1|0;	sbit x=P1*0;
In 8051, each register bank has _____ registers.	2	4	8	16
8051 has _____ bytes of general-purpose data memory.	64	60	80	128
A pinout of the 8051 packaged in a _____ pin DIP.	4	8	32	40
The program counter (PC) and the data pointer (DPTR) are _____ bit registers.	32	4	8	16
The B register is used with the A register for _____ and _____ operations.	Multiplication, division	Addition, subtraction	Multiplication, addition	Division, subtraction
8051 microcontrollers have a _____ bit addressing bus.	16	32	64	128
If EA=_____, the microcontroller completely ignores internal program memory and executes only the program stored in external memory.	0	1	2	3
If EA=_____, the microcontroller executes first the program from built-in ROM,	0	1	2	3

then the program stored in external memory.				
In 8051 Register Bank address is _____.	00h to 1Fh	20h to 2Fh	30h to 7Fh	30h to 70h
In 8051, bit addressable area is _____.	00h to 1Fh	20h to 2Fh	30h to 7Fh	30h to 70h
In 8051 general purpose RAM address is _____.	00h to 1Fh	20h to 2Fh	30h to 7Fh	30h to 70h
In C programming, an 8-bit unsigned char ranges from _____.	-128 to +127	0 to 255	-127 to 128	0 to 256
In C programming, an 8-bit signed char range from _____.	-128 to +127	0 to 255	-127 to 128	0 to 256
In C programming, an 16-bit unsigned integer ranges from _____.	-32768 to +32767	0 to 65535	-32767 to 32767	0 to 65536
In C programming, a 16-bit signed integer range from _____.	-32768 to +32767	0 to 65535	-32767 to 32767	0 to 65536
Size of sbit is ____ bit.	32	8	16	1
Size of SFR is ____ bit.	1	8	16	32
0x35 & 0x0F =_____.	0x35	0x30	0x05	0x0F
0x04 | 0x 30 = _____.	0x00	0x43	0x34	0x04
Select a valid packed BCD number.	0xA0	**0x95**	0x0A	0xF0
0x54^0x54=_____.	0x00	0x54	0xFF	0x45
~0xAA= _____.	0x55	0xAA	0xFF	0x00
~0xFF= _____.	0x55	0xAA	0xFF	0x00
ASCII 30h represent digit/key _____.	0	1	2	3
The code for every embedded program is written in an _____ loop.	Infinite	Finite	For	While
The process which converts source code to executable code is called as the _____ process.	Link	Locate	Debug	Build
Simulator only simulates the _____.	processor	Input	Output	GUI
A compiler which produces the executable code to be run on a different platform is called a _____.	Compiler	cross-compiler	Linker	Cross Linker
The process of compiling is done by the _____.	Linker	Compiler	Cross compiler	Cross Linker
The compiler takes input as source code files and gives output as _____ object files.	1	2	5	Multiple
_____ section describes the sections that will be contained in the object file.	header	text	data	bss
_____ section contains all code blocks.	Header	Text	Data	Bss

_____ section contains all initialized global variables and their values	Header	Text	Data	Bss
_____ section contains all un-initialized global variables.	Header	Text	Data	Bss
The process of linking is carried out by the _____.	Compiler	Linker	Cross compiler	Cross Linker
The linker takes input as multiple object files and gives output as a single object file which is also called as the ____ code.	Executable	Hex	Machine	Relocatable
The job of the _____is to combine multiple object files and resolve the unresolved symbols.	Compiler	Cross compiler	Linker	Cross Linker
The process of relocating is carried out by the____.	Compiler	Linker	Relocater	Cross-Relocator
The relocater takes input as the relocatable code produced by the linker and gives output as the final _____ code.	Relocatable	Executable	Object	C
The output of build process is a binary executable file which is called _____ code.	Relocatable	Hex	Object	C
The process of putting this code in the memory chip of the target embedded system is called_____.	Installing	Compiling	Building	Downloading
A device programmer is a piece of _____.	Hardware	Software	Program	Processor
_____ is the process of eliminating the bugs/errors in software.	Debugging	Compiling	Building	Locating
The most primitive method of debugging is using _____.	Stepper motor	Buzzer	Button	LED
A _____ contains a hardware interface between the host computer and the target embedded system.	Remote Debugger	Remote control	Simulator	Emulator
A _____ can be quite valuable in the earlier stage of a project when there has not yet been any actual hardware implementation for the programmers to experiment with.	Remote Debugger	Remote control	Simulator	Emulator
A _____ is a completely host-based program that simulates the functionality and instructions set of the target processor.	Remote Debugger	Remote control	Simulator	Emulator
The ROM ____ is a true replacement for the original ROM	Remote Debugger	Emulator	Remote control	Simulator

The ROM _____ has its own serial or network connection to the host.	Remote Debugger	Remote control	Simulator	Emulator
Emulator uses a remote debugger for its human interface.	Remote Debugger	Remote control	Simulator	Emulator
Communication between the GDB frontend and debug monitor is _____-oriented and designed for transmission over a serial connection.	Byte	Char	Bit	Stream
_____ provides for low-level control of the target processor and is usually called the debug monitor.	Backend remote debugger	Frontend remote debugger	Simulator	Emulator
The Software interface of the _____ has GUI-based main window and several smaller windows for the source code, register contents and other information about the executing program.	Remote control	Simulator	Emulator	Remote Debugger
Frontend remote debugger runs on the _____.	host computer	guest computer	target host	target processor
_____ remote debugger provides the human interface.	Backend	Frontend	Simulator	Emulator
_____ remote debugger runs on the target processor.	Frontend	Simulator	Backend	Emulator
Debug monitor is a piece of _____ that has been designed specifically for use as a debugging tool for processors and chips.	Software	Hardware	Processor	Input
_____ is a piece of laboratory equipment that is designed especially for troubleshooting digital hardware.	Logic Simulator	UART	Buffer	Logic Analyzers
_____ can have multiple inputs (up to 100 even), each capable of detecting whether the electrical signal it is attached to is currently at logic level 1 or 0.	Logic Analyzers	Logic Simulator	UART	Buffer
COFF stands for _____.	Center object file format	Compiling object file	Common Oriented file	Common Object File Format
The job of _____ is mainly to translate human readable program into equivalent set of opcodes.	Compiler	Linker	Cross compiler	Cross Linker
Which development tool / program has the potential to allocate the specific addresses so as to load the object code into memory?	Loader	Locator	Library	Linker
COFF is also known as _____	executable file	hex code	C# code	Primary code

The code to be run on the target embedded system is called as _____	binary executable code	C# code	Primary code	Native code
A _____ can be used to download, execute and debug embedded software over a serial port or network connection between host and target.	Cross Compiler	Remote Linker	Remote Debugger	Remote compiler
What does ICE stand for?	in-circuit emulation	in-code EPROM	in-circuit EPOM	in-code emulation
Which of the following is a traditional method for emulating the processor?	SDS	ICE	CPU simulator	Low-level language simulator
_____ is use to downloading the binary image on the embedded system	Device Programmer	Simulator	CRO	Logical Analyzer
_____ is use to downloading the binary image on the embedded system	Simulator	CRO	Logical Analyzer	In system programmer
A debug monitor is also called as _____	RAM Monitor	ROM Monitor	target Monitor	None of these
A_____ is a piece of laboratory equipment designed specifically for troubleshooting digital hardware.	Emulators	Simulators	logic analyzer	Remote Debugger
_____ can be used as a starting program in embedded system.	Hello world	Blinking LED	7 segment display	stepper motor
CRO stands for _____	Cathode Ray Oscilloscope	Current Resistance Oscillator	Central Resistance Oscillator	Capacitance Resistance Oscilloscope
C.R.O gives _____	actual representation	visual representation	approximate representation	incorrect representation
The information about a task is recorded in a data structure called the _____.	task context	Context Switch	Context Awareness	Context Monitor
An IDE also known as _____	Integrated design environment	Integrated debugging environment	Integral design environment	Integrated development environment
A transition of state between the ready and running state occurs whenever the operating system selects a _____ to run.	new task	old task	terminated task	aged task
The heart and soul of any operating system is its _____.	Scheduler	Kernel	User Application	Monitor
_____ scheduling uses algorithms that allow every task to execute for a fixed amount to time.	Shortest job first	Priority	Round robin	First come first serve
A running task is interrupted an put to a _____ state if its execution time expires.	Interrupted	New	Terminated	Waiting

The scheduling points are the set of operating system events that result in an invocation of the _____.	Kernel	Scheduler	User Application	Monitor
A _____ point called the clock tick is a periodic event that is triggered by a timer interrupt.	Waiting	Terminating	Scheduling	Interrupt
The ready list is implemented as an ordinary _____, ordered by priority.	linked list	class	heap	object
If there are no tasks in the ready state when the scheduler is called, the _____ task will be executed.	Normal	Idle	Process	Wait
The actual process of changing from one task to another is called _____.	Context Monitoring	Context Awareness	Context Switch	Swapping
Mutexes are mechanisms provided by many operating systems to assist with _____.	task creation	task synchronization	task deletion	task termination
A mutex is a multitasking-aware _____.	unary flag	binary flag	ternary flag	Universal flag
An OS is said to be _____ if the worst-case execution time of each of the system calls is calculable.	Deterministic	Non-deterministic	Soft-Real Time	Inexpensive
_____ is the total length of time from an interrupt signal's arrival at the processor to the start of the associated interrupt service routine.	Interrupt time	Read Time	RTT	Interrupt Latency
Operating Systems that offer only a basic scheduler and a few other system calls are _____.	Inexpensive	expensive	Rare	Free
_____ contains an information about the cross compilation process like cross compiler details, formatted source text('C' code), assembly code generated from the source file, symbol tables, errors and warnings detected during the cross-compilation process.	Map File	List File	Hex file	Object File
The tool used for converting and object file into a hex file is known as object to _____.	Assembler	Compiler	Hex converter	Debugger
A _____ is a reverse engineering tool	Debugger	Assembler	Compiler	Disassembler
A DISASSEMBLER is a utility program which converts _____ codes into target processor specific _____ code/instruction.	Machine, Assembly	high level, Machine	Assembly, high level	Machine, Object

A DECOMIPILER is a utility program for translating _____ codes into corresponding _____ language instruction.	high level, Machine	Source, high level	Machine, Object	Machine, high level
EDLC is Embedded Product Development Life Cycle	Embedded Product Design Life Cycle	Embedded Development Life Cycle	Embedded Process Development Life Cycle	Embedded Product Development Life Cycle
The _____ identifies application environment and creates an overall architecture for the product.	development phase	design phase	retirement phase	support phase
_____ transforms the design into a realizable product.	Development phase	Design phase	Retirement phase	Support phase
The _____ ensures that the product meets the user needs and it continues functioning in the production environment.	Development phase	design phase	Retirement phase	support phase
_____ is the process of launching the first fully functional model of the product in the market.	Deployment	Design	Retirement	Support
The _____ deals with the operational and maintenance of the product in the production environment.	Retirement phase	support phase	Development phase	design phase
_____ is the final phase in a product development life cycle where the product is declared as discontinued from the market.	Retirement phase	support phase	Development phase	design phase
_____ is the one adopted in most of the olden systems.	Waterfall model	Prototyping model	Spiral model	Iterative model
In waterfall model, the fixes for the bug are postponed till the _____.	support phase	Retirement phase	Development phase	design phase
Today's processors with _____ technology can pack together ten of thousands of IC/gates per processor.	Very Large-Scale Integration (VLSI)	Small Scale Integration (SSI)	Medium Scale Integration (MSI)	Normal Scale Integration (NSI)
Today's processors are capable of achieving execution frequency in rage of _____.	KHz	MHz	GHz	PHz
In Dual Core processor has _____ cores.	1	2	3	4
Quad processor has _____ cores.	1	2	3	4
Java programs are compiled by a compiler into _____.	Bytecode	Hex code	Executable code	Machine code
_____ is a replacement of the original .NET framework to be used on embedded systems.	.NET CF	JVM	CLI	ASP
The rate at which processors can process may have increased considerably but rate at which	faster	slower	moderate	not measurable

memory speed is increasing is _____.				
Standards in the embedded industry are followed only in certain handful areas like _____.	Robotics	Home automation	Mobile handsets	CCTV
_____involves understanding what product needs to be developed.	Analysis	Design	Implementation	Testing
_____ involves what approach to be used to build the product.	Analysis	Design	Implementation	Testing
The _____ is the repetitive process in which the Waterfall model is repeated over and over to correct the ambiguities observed in each iteration.	Spiral Model	Waterfall model	Prototyping Model	Iterative model
Embedded systems are being designed on single silicon chip called as _____.	SSC	SoC	SCC	SCO
OMA stands for_____ .	opcode mobile alliance	object mobile alliance	open mobile alliance	open media alliance
_____ is a single board microcontroller, proposed to make the application of interactive objects.	DSP	Arduino	ASIP	SoC
Which of the following is not the state of a task?	New	Old	Waiting	Running
Process synchronization of programs is done by _____	input	output	operating system	memory
Which algorithm is defined in Time quantum?	shortest job scheduling algorithm	round robin scheduling algorithm	priority scheduling algorithm	multilevel queue scheduling algorithm
What is a short-term scheduler?	It selects which process has to be brought into the ready queue	It selects which process has to be executed next and allocates CPU	It selects which process to remove from memory by swapping	It selects a process that has to be added into memory by swapping
What is a long-term scheduler?	It selects which process has to be brought into the ready queue	It selects which process has to be executed next and allocates CPU	It selects which process to remove from memory by swapping	None of the mentioned
Hex processor has _____ cores.	6	66	4	8