

PUNE VIDYARTHI GRIHA'S

Affiliated to University of Mumbai

COLLEGE OF SCIENCE AND TECHNOLOGY

Question Bank

Class: F.Y.B. Sc.IT Semester: II

Subject: Microprocessor Architecture

Sr	Question	A	В	С	D
no					
	Microprocessor was introduced				
1	in the year	1945	1971	1974	1980
	Flip – flops are used in a				
	microprocessor to				
2	indicate	Shift register	latches	counters	flags
	The number of address lines				
	required to access 64 Kbyte of				
	memory of the microprocessor				
3	is	16	32	20	8
	Flip –flops are used in a				
	microprocessor to				
4	indicate	shift register	latch	counters	flag
	The first microprocessor				
5	was Which of the following	4001	8085	4003	4004
	microprocessor has an 8 bit data				
6	bus	4004	80186	8085	8086
	The number of flags in 8085				
7	are	4	8	6	5
	A microprocessor			an analog and	
8	is	an analog device	a digital device	digital device	hybrid device
	The 16 bit processor				
9	is	8085	8086	80486	pentium
				unidirectional	
	The data bus of microprocessor			as well as bi	semi -
10	is	unidirectional	bi –directional	directional	directional
	Which system communicates				
	with the outside word via the	3.61	3.5	Digital	Hybrid
11	I/O devices interfaced to it:	Microprocessor	Microcomputer	computer	computer
1.0	How many generation of		771	a.	TT.
12	microprocessor?	Four	Five	Six	Three
	Each machine cycle consists of				
1.0	many clock periods called		instruction	6 . 1 . 1	
13	as	t-states	cycle	fetch cycle	machine cycle
1.4	The length of LXI H, 9000H is	1 .		.1 1 .	6 1 .
14	·	one-byte	two-byte	three-byte	four-byte

l 1		Ì	İ		l 1 0005 l
		1 0005	1 0005	1	because 8085
	W/h 0005	because 8085	because 8085	because 8085	processor has
15	Why 8085 processor is called an 8 bit processor?	processor has 8 bit ALU	processor has 8 bit data bus	processor has 16 bit data bus	16 bit address
13		DIL ALU	on data bus	10 bit data bus	bus
16	The address / data bus in 8085	multiplayed	demultiplexed	decoded	encoded
10	is In 8085 name the 16 bit	multiplexed	•	Instruction	encoded
17		Accumulator	Program	decoder	ALU
1 /	registers? pin of 8085 is useful for	Accumulator	counter	decodei	ALU
18	interfacing low speed devices.	Doody	RIM	ALE	SIM
10	interfacing fow speed devices.	Ready	Operation code	ALE	SIM
	Machine language instruction	Operation code	field & operand		none of the
19	format consist of	field	field	Operand field	mentioned
19		Held	Heiu	Operand field	None of these
20	Assembly language programs are written using	Hex code	Mnenonics	ASCII code	View
20		Hex code	Milenomes	ASCII code	View
21	How many types of Interfacing does a microprocessor have?	2	3	4	5
21	<u> </u>		3	4	3
22	Which of the following are known as Higher Address Bus?	A15 - A8	AD7 - AD0	READY	WR
22	kilowii as Higher Address Bus?	A13 - A0		Device	W K
		Diamlary Mamany	Directly	Memory	Direct Mamore
23	DMA stands for?	Display Memory Access	Memory Access	Access	Direct Memory
23	DIVIA stands for?	It has three	Access	Access	Access
			Eash shownst	Eagle alsound	Dook shound
		channels which can be used over	Each channel has 16-bit	Each channel can transfer	Each channel can be
	Which of the following is not	three I/O	address and 14-		
24	Which of the following is not true features of 8257?			data up to	programmed
24		devices.	bit counter.	64kb.	independently.
25	A microprocessor instruction set can be classified into?	2	3	4	5
23	Microprocessor 8085 is a	<u> </u>	3	_	3
26	bit processor.	4	8	16	32
20	There are address	т	0	10	32
27	lines in Microprocessor 8085.	4	8	16	32
21	The data bus consists of	т	0	10	32
28	lines.	4	8	16	32
20	bus is bi-	_	0	10	32
29	directional.	Data	Address	Control	Memory
2)	Register is part of	Data	Address	Control	Wichiory
30	ALU.	A	В	С	D
50	Register A is of	11	U U		<i>D</i>
31	bits in Microprocessor 8085.	4	8	16	32
51	Each instruction has two parts:	'		10	32
	one is task to be performed,				
32	called the	opcode	operand	Instruction	mnenonics
	Each instruction has two parts:		- F - 1 - 1 - 1 - 1		
	one is data to be operated on				
33	called the	opcode	operand	Instruction	mnenonics
	A instruction	- p	- P		
	includes the op-code and				
34	operand in the same byte.	one-byte	two-byte	three-byte	four-byte
	In a three-byte instruction, the	,	, , , ,	<i>J</i> · ·	, , , ,
	first byte specifies				
35	the	opcode	operand	Instruction	mnenonics
36	In a three-byte instruction, the	opcode	lower order	lower order	higher order
50	in a directory to instruction, the	ореоне	10 HOL OLUCI	10 WEI OIGEI	inglier order

	second byte specifies		address	address or data	address
	the In a three-byte instruction, the				
	third byte specifies		lower order	higher order	higher order
37	• •	onaoda	address	higher order address or data	address
37	the	opcode	address	address of data	address
	In a two-byte instruction, the				
20	second byte specifies			T.,	
38	the	opcode	operand	Instruction	mnenonics
	is defined as the time				
	interval between 2-trailing or		instruction		
39	leading edges of the clock.	t-states	cycle	fetch cycle	machine cycle
	The total time required to				
	execute an instruction given				
40	by	IC = Fc - Ec	IC = Fc + Ec	IC = Fc + Mc	IC = Mc + Ec
	Low level computer language	Assembly	Programming	Machine	
41	are also called as	language	language	language	mnenonics
	Middle level computer				
	language are also called	Assembly	Programming	Machine	
42	as	language	language	language	mnenonics
	are high-speed				
	computers, and their word				
	length generally ranges from 32				
43	to 64 bit.	Large computer	Mainframe	Medium size	Microcomputer
	operation accepts data				
44	from input devices.	Memory Read	Memory Write	I/O read	I/O Write
	operation sends data to	•	_		
45	output devices.	Memory Read	Memory Write	I/O read	I/O Write
	Microprocessor 8085 can	·	•		
	operate on clock cycle with				
46	% duty cycle.	20	40	50	60
	This is a +ve pulse generated				
	every time when 8085 begins				
	an operation(machine cycle); it				
	indicates that the bits on AD0 –				
47	AD7 are address bits.	RD	WR	ALE	HOLD
	When the signal on this pin				
	goes low, the program counter				
	is set to zero the buses are tri-				
48	stated and the MPU is Reset.	RD	RESET OUT	ALE	RESET IN
	Having received				
	request the microprocessor				
	relinquishes the use of the buses				
	as soon as the current machine				
49	cycle is completed.	Ready	RESET OUT	ALE	RESET IN
7/	The data on this line is loaded	Ready	KLDLI OUI	THE	ICEDET IIV
	into accumulator whenever a				
50	RIM instruction is executed.	Ready	RIM	ALE	SIM
50	STA 4000 isbyte	Roudy	KIIVI	71111	DIM
51	instruction.	one	three	two	four
51	RAL is an example of	Offic	unce	two	1001
52	addressing mode.	register	direct	implied	immediate
54	Stack pointer is a	10813101	direct	mpneu	miniculate
53	register.	16 bit	8 bit	32 bit	4bit
				JZ UIL	
54	In memory mapped I/O device	8bit address	IN		OUT

	is identified by		instruction16bit address		instruction
55	In I/O mapped input device	latch	buffer	decoder	stools
33	is	laten	buller	decoder	stack
56	In I/O mapped output device is	buffer	encoder	latch	stack
	If accumulator content is 88H, after execution of CMA accumulator content will				
57	be	77H	93H	FFH	80H
58	LDA isInstruction.	arithmetic	logical	branch	data transfer
	If A=56H,B=82H after		C		
	execution of ANA B, content of				
59	A=	02H	56H	00H	D8H
	8085 has EPROM				
60	of	1Kb	526bytes	64kb	256 bytes
	In 8085, 16-bit address bus,	1.000	2217	CATTE	100775
61	which can address upto?	16KB	32KB	64KB	128KB
	There are general				
62	purpose registers in 8085 processor.	5	6	7	8
02	It is also a 16-bit register works	3	0	,	0
	like stack, which is always				
	incremented/decremented by 2		Temporary		Program
63	during push & pop operations.	Stack pointer	register	Flag register	counter
	Flag register is an 8-bit register	-			
64	having 1-bit flip- flops.	3	4	5	6
04	порв.	3	4		It is a 16-bit
		It is an 8-bit	When an		register used to
		register, which	instruction is		store the
		holds the	fetched from	It provides	memory
		temporary data	memory then it	timing and	address location
		of arithmetic and	is stored in the	control signal	of the next
	What is true about Program	logical	program	to the	instruction to be
65	counter?	operations.	counter	microprocessor	executed.
	This signal indicates that				
	another master is requesting the use of the address and data				
66	buses.	READY	HOLD	HLDA	INTA
00	This signal is used as the	KL/ID I	HOLD	TILDI	111111
	system clock for devices				
	connected with the				
67	microprocessor.	X1, X2	CLK OUT	CLK IN	IO/M
		These signals are	There are 3	Three status	
	Which of the following is true	used to identify	control signal	signals are	
	about Control and status	the nature of	and 3 status	IO/M, S0 &	
68	signals?	operation.	signals.	S1.	All of the above
	The register in the 8085A that				
	is used to keep track of the memory address of the next op-				
	code to be run in the program is		program	instruction	
69	the:	stack pointer	counter	pointer	accumulator
70	The data bus in 8080A/8085	eight	sixteen	eight	eight lines used
, 0	1110 aata 045 111 0000/1/000J	Cigin	SIACCII	CISIII	orgin innes used

	microprocessor is a group of	bidirectional lines that are used to transfer 8 bits between the microprocessor and its I/O and memory	bidirectional lines that are used for data transfer between the microprocessor and memory	unidirectional lines that are used for I/O devices	to transfer data among the registers
	In 8085, to disable the whole	the DI	the DO	the INTERRUPT	the El
	interrupt system (except	instruction may	instruction may	instruction	instruction may
71	TRAP).	be used	be used	may be used	be used
	Exceptions to the 8085				jump
	microprocessor normal	jump		_	instructions or
72	operation are called:	instructions	decoding	interrupts	interrupts
	In 8085 microprocessor, which				
73	of the following interrupts has the highest priority?	RST 5.5	RST 7.5	TRAP	INTR
13	Which of the following was not	K31 3.3	KS1 7.3	Arithmetic	INTK
	a design improvement for the	Execution unit		logic unit	Bus interface
74	8086/8088 over the 8085?	(EU)	16-bit data bus	(ALU)	unit (BIU)
	How many buses are connected	\ - /		\ -/	\ -/
	as part of the 8085A				
75	microprocessor?	2	3	5	6
	Register A is of				
76	bits in Microprocessor 8085.	4	8	16	32
	All the arithmetic and logic				
	operations are done considering				
77	as one of the operand register.	A	В	С	D
7.7	Program counter register of	A	В		D
	Microprocessor 8085 is of				
78	bits.	4	8	16	32
	One of the following register is				
79	of 16-bits.	D	Е	F	SP
80	One of the following is not a Register of Microprocessor 8085.	E	C	L	F
	instruction transfers				
	the contents from Reg A to Reg				
81	В.	MOV A,B	MOV B,A	ADI B	ADI A
0.0	Register is a part of		.	<u> </u>	5
82	ALU.	A	В	С	D
	After any arithmetic or logic operation the result is generally				
83	stored in Register.	Н	L	F	A
0.5	The instruction for comparing	11	L	1	11
84	the contents of register is.	CMA	CMP	CPM	CPI
	There are Rotate				
85	instructions in 8085.	2	3	4	5
	The rotate instruction rotates				
86	the contents of Register.	A	В	С	D
0.5	One of the following is an	1.5	200	22	***
87	invalid register pair.	AB	BC	DE	HL
88	To address a memory chip	8	9	10	11

	having 1024 registers				
	address lines are used.				
00	The total memory capacity of	2217	6.417	10017	510X
89	8085 is bytes.	32K	64K	128K	512K
	For a microprocessor based				
00	system the system performance	A 11 D	D (D	G . 1D	A 11 D
90	is given by.	Address Bus	Data Bus	Control Bus	All Bus
	For a microprocessor based				
0.1	system the system capacity is	A 11 D	D (D	G . 1D	A 11 D
91	given by	Address Bus	Data Bus	Control Bus	All Bus
	The instruction adds				
0.2	the contents of Reg A with Reg	4 DD 4	ADD C	ADD C A	ADDAG
92	C in 8085.	ADD A	ADD C	ADD C,A	ADDA,C
	The memory location in MOV				
02	A,M is pointed by	D.C.	DE	111	DE
93	register pair.	BC	DE	HL	BE
0.4	One of the following is an	CITA X/A	IDAND	CTAVD	IDAVD
94	invalid instruction of 8085.	STAX A	LDAX B	STAX D	LDAX D
	One of the following is not a				
0.5	valid register pair in	AD	D.C.	DE	111
95	8085	AB	BC	DE	HL
06	The instruction LXI H, 1020 is	1	2	3	4
96	a byte instruction.	1	2	3	4
07	One of the following is 2 byte	A DI 12	IDAVD	CTAVD	MOVMA
97	instruction One of the following is a logic	ADI 12	LDAX B	STAX D	MOV M,A
00	One of the following is a logic	ADD A	ANIAD	CLID C	DCD C
98	instruction	ADD A	ANA B	SUB C	DCR C
	There are				
00	conditional jumps in	4	(7	8
99	8085	4	6	7	8
	One of the following represents				
100	an umconditional jump in 8085	INC	JZ	JM	JMP
100		JNC	JZ.		JIVIP
	In which of these modes, the	manistan anamand	immediate	register and	none of the
101	immediate operand is included	register operand		immediate	none of the
101	in the instruction itself?	mode	operand mode	operand mode	mentioned
	A sequence of two registers that multiplies the content of DE				
	register pair by two and stores				
	the result in HL register pair (in				
	8085 assembly language) is	XCHG & DAD	XTHL & DAD	PCHL & DAD	XCHG & DAD
102	ooos assembly language) is	B	H H	D D	H
102	The accumulator contains 85H,	מ	11	ע	11
	register B contains 68H, what is				
	the content of accumulator and				
	CY (carry) after executing the				
	following code?				
	ADD B				
103	DAA	35H, 1	53H, 0	35H, 0	53H, 1
103	Which instruction is required to	3311, 1	3311, 0	3311, 0	JJ11, 1
	rotate the content of				
	accumulator one bit right along				
104	with carry?	RLC	RAL	RRC	RAR
105	The accumulator contains 03H	83H, 0	38H, 0	83H, 1	38H, 1

1 1	and ragistar D containd 81U				1
	and register D containd 81H, what is the content of the				
	accumulator and the CY after				
	executing ORA D?				
	Register pair used to indicate				
106	memory	B and C	D and E	H and L	W and Z
107	What are software interrupts?	RST 0-7	RST 5.5 - 7.5	INTR, TRAP	RST 4.4 - 6.4
107	For one's complement	110107	101010 710	21 (114, 114, 1	1101 0
108	following instruction is use.	CMA	CMP	CMC	CMT
	For Exchanging data following				
109	instruction is used.	Exchange	XCHG	Change	EXCH
	Checking for errors in the				
	program by observing the				
	execution of instruction is			Dynamic	
110	·	Static debugging	Reg debugging	debugging	A & C
	The time required for the				
	execution of the program		instruction		
111	depends on	t-states	cycle	fetch cycle	machine cycle
110	instruction use to adjust	DAD	DDA	DAA	A.D.A
112	result to BCD.	DAD	DDA	DAA	ADA
	CMA	aalaylata 1'a	aalaulata 2'a		
113	ADI 01H	calculate 1's	calculate 2's	addition	aammlamant
	above code will perform.	complement	complement		complement
114	DAD B means	HL+BC	H+B	L+C	D+B
115	SBB B instruction says	A-B-Borrow	B-B	B-B-Borrow	A & B
	The accumulator contains 77H				
	and register D containd 56H,				
	what is the Content of the				
116	accumulator and the CY after executing XRA D?	21H, 1	12H, 0	21H, 0	12H, 1
110	executing ARA D:	MVI D, Count	MOV D, Count	MVI D, Count	MOV D, Count
	To generate a delay using 8 bit	L1: DCR D	L1: DCR D	L1: DCX D	L1: DCX D
117	counter	JNZ L1	JNZ L1	JNZ L1	JNZ L1
117	What is the length of the	V1 (2 21	VI (2 21	V1 (2 21	011221
	temporary register of 8085				
118	microprocessor?	32 bits	12 bits	16 bits	8 bits
	How many I/O ports can be				
	accessed by direct method in				
119	8085 microprocessor?	8	128	256	64
	What is the addressing mode				
	used in instruction MOVE M, C				
120	?	Direct	Induced	Indirect	Immediate
	What addressing mode is used				
121	in the instruction LDA 0345H?	Direct	Implied	Indirect	Immediate
	The accumulator contains 39H,				
	register C contains 12H, what is				
	the content of accumulator and				
122	CY (carry) after executing the	05H, 1	50H 1	51U A	5011.0
122	following code? Two 8-bit temporary registers	USA, I	50H, 1	51H, 0	50H,0
123	of 8085 microprocessor?	В & С	D & E	W & Z	H & L
143	Registers exclusively used for	Dac	Dar	W & Z	II & L
124	the internal operation by the	В & С	D & E	W & Z	H & L
147	the internal operation by the	Dac	Dal	11 & L	II & L

	microprocessor				
	This instruction copies H and L				
	register to the stack pointer				
125	·	SPHL	XTHL	CPHL	HLSP
	This instruction exchanges H				
	and L with top of stack				
126		SPHL	XTHL	CPHL	HLSP
	 '		Copy data from	_	Copy from i/p
		Copy data from	Accumulator to		device with
		i/p to device	o/p device with	Copy F8 to	address F8 to
127	Outcome of OUT F8H .	with address F8	address F8	Output port	Accumulator
127	ADD B is a byte	With address 1 o	uddi ess i o	output port	1 100 dillidiator
128	instruction.	1	2	3	4
120	mstraction.	1	2	Load contents	Т
				of A into	
		Load contents of	Load contents	memory	Load contents
		memory location	of I/O location	location	of A into I/O
129	LDA 2050H will	2050H into A	2050H into A	2050H	location 2050H
147		203011 III.U A	203011 IIIU A	Jump on	100001011 202011
130	JP stands for	Jump on Parity	Jump on Plus	Positive	Jump on Prime
130	JI Stands IOI	Jump on Lamy	Jump on Fius	Copies	Jump on Finne
		is an incorrect	copies data into	_	None of the
131	LDAX C .	instruction	Accumulator	memory location	above
131	A = AAH. CY = 0. On	ilistruction	Accumulator	iocation	above
132	executing RLC. A will become	4511	55H	ВВН	AAH
132	·	45H Divide	Decimal	ррп	ААП
	DAA command stands for	Accumulator	Accumulator	Divida Adinat	Dagimal Adjust
133	DAA command stands for	Arithmetic	Arithmetic	Divide Adjust Accumulator	Decimal Adjust Accumulator
133	·				
		Logical AND register B with	Logical AND	Logical AND register B with	Logical AND
134	ANA B will	the accumulator	register B with B	_	register B with
134	ANA B WIII	the accumulator	Logical AND	i/p	o/p
		Logical AND	•		Logical AND
		C	immediate port address 01	Laciaal AND	Logical AND
		immediate 01		Logical AND	immediate
125	A N.H. O.1:11	with the	with the	immediate 01	accumulator
135	ANI 01 will	accumulator	accumulator	with 01	with itself
		Evaluaiva OP	OP mamam:	Exclusive OR	OP M Pagistar
		Exclusive OR	OR memory	M register with	OR M Register
126	VD A M:11	memory with the	with the	the	with the
136	XRA M will	accumulator	accumulator	accumulator	accumulator
		Datum fra 11-	Return from	Datum f	Dotum from 41
		Return from the	the subroutine	Return from	Return from the
127	Instruction DDE 111	subroutine if	if parity flag is	the subroutine	subroutine if
137	Instruction RPE will	parity flag is 0	D-4 C	if Positive	Prime
		Returns from the	Returns from	Returns from	Returns from
120	Landana di DAK 111	subroutine if	the subroutine	the subroutine	the subroutine
138	Instruction RM will	sign flag is 0	if mean is 1	if sign flag is 1	if minus is 1
120	Push value of accumulator and	OTTA OTZ ET A CC	PUSH	PUSH	DIJOH DOM
139	flag in stack.	STACK FLAGS	FLAGS,A	A,FLAGS	PUSH PSW
		D 1 6		Pop value from	
		Pop value from	D 1 2 2 2	bottom of	ъ .
1.40	DODAY	TOP of memory	Pop value of H	memory stack	Pop value
140	POP H.	stack in H	to Accumulator	in H	memory in H

times will DCR B Instruction get executed? MVI B.FFHLOOP: DCR B JNZ LOOP RET 256 255 128 512 JNZ LOOP RET 256 255 128 512 JNZ LOOP Will require how many t-states? 10 14 12 6 Rotate accumulator left through carry without carry SHLD us a byte instruction will Store HL registers Direct Indirect I	1 1	In the below code, how many]]	1
get executed? MVI B,FFHLOOP. DCR B JNZ LOOP RET 256 255 128 512						
B.FFHLOOP: DCR B						
141 LOOP RET 256 255 128 512 142 JNZ LOOP will require how many t-states? 10 14 12 6 Rotate accumulator left without carry SHLD us a byte instruction will Store HL registers Indirect Set the Carry Subtract the Carry Exchange Exchange Exchange Contents of HL & DE & Exchange Contents of HL & SP & SP & SP & SE &		C				
JNZ LOOP will require how many t-states?	141	· · · · · · · · · · · · · · · · · · ·	256	255	128	512
142 many t-states?						
Rotate accumulator left description Rotate all left without carry Rotate all left withou	142	•	10	14	12	6
Rotate accumulator left without carry Rotate all left through carry SHLD us a byte Ishtruction. 1						
RAL instruction will byte 1			Rotate			
RAL instruction will byte SHLD us a byte instruction.					Rotate all left	Rotate all left
SHLD us a byte instruction.	143	RAL instruction will .				
SHLD instruction will			<u>U</u>	,	<u> </u>	
SHLD instruction will Store HL registers registers registers registers Indirect Ind	144		1	2	3	4
Table create Table fold Table look-up						Store into HL
Table create Table fold Table look-up		SHLD instruction will	Store HL	registers	registers	registers
Copy H & L registers into Program counter. HLPC Set the Carry Subtract the Carry Accumulator Exchange Exchange Exchange Contents of HL & DE & Exchange Exchange Contents of HL & DE & Exchange Exchange Contents of HL & SP	145			•		_
146		Copy H & L registers into				-
Set the Carry Flag Contents Carry Accumulator	146		HLPC	PCHL	CPHL	CPPC
STC will Flag						
Exchange contents of HL & DE & PC & Exchange contents of HL & DE & PC & & HL & & SP &	147	STC will .	•			
Contents of HL & DE & DE & PC & HL & SP				Exchange	-	Exchange
is a valid Maskable interrupt. RST 8.5 TRAP RST 5.5 RST 4.5 When a BCD number is to be displayed by a seven-segment led, it is necessary to the BCD number to its seven-segment code. Convert Ordered Arrange Delete In the technique, the codes of digit to be displayed are stored sequentially in memory. Table assign Table create Table fold Table look-up The conversion program located the code of a digit based on its magnitude and transfer the code to the MPU to send out to a Input port display port HDD RAM The American standard code for is used community in data community in data community in data communication. information information information interchange inter				_		
is a valid Maskable interrupt. RST 8.5 TRAP RST 5.5 RST 4.5 When a BCD number is to be displayed by a seven-segment led, it is necessary to the BCD number to its seven-segment code. Convert Ordered Arrange Delete In the technique, the codes of digit to be displayed are stored sequentially in memory. Table assign Table create Table fold Table look-up The conversion program located the code of a digit based on its magnitude and transfer the code to the MPU to send out to a Input port display port HDD RAM The American standard code for is used community in data community in data communication. information information information interchange interchang	148	XCHG will .	& DE	& PC	& HL	
When a BCD number is to be displayed by a seven-segment led, it is necessary to the BCD number to its seven-segment code. Convert Ordered Arrange Delete In the technique, the codes of digit to be displayed are stored sequentially in memory. Table assign Table create Table fold Table look-up The conversion program located the code of a digit based on its magnitude and transfer the code to the MPU to send out to a Input port display port HDD RAM The American standard code for is used community in data information information information information intrachange interchange interchange interchange interchange 154 ASCII is a code. seven-bit six-bit five-bit four-bit		is a valid Maskable				
When a BCD number is to be displayed by a seven-segment led, it is necessary to the BCD number to its seven-segment code. Convert Ordered Arrange Delete In the technique, the codes of digit to be displayed are stored sequentially in memory. The conversion program located the code of a digit based on its magnitude and transfer the code to the MPU to send out to a Input port display port HDD RAM The American standard code for is used community in data community in data communication. intrachange interchange	149	interrupt.	RST 8.5	TRAP	RST 5.5	RST 4.5
displayed by a seven-segment led, it is necessary to the BCD number to its seven-segment code.		When a BCD number is to be				
led, it is necessary to the BCD number to its seven-segment code.						
BCD number to its seven- segment code. In the technique, the codes of digit to be displayed are stored sequentially in memory. Table assign Table create Table fold Table look-up The conversion program located the code of a digit based on its magnitude and transfer the code to the MPU to send out 152 To a Input port The American standard code for is used community in data community in data information intrachange interchange 154 ASCII is a code. Seven-bit Ordered Arrange Delete Table fold Table look-up Table create Table fold Table look-up Table create Table fold Table look-up Table look-up Table create Table fold Table look-up Input port HDD RAM						
In the technique, the codes of digit to be displayed are stored sequentially in memory. Table assign Table create Table fold Table look-up Table look-up Table create Table fold Table look-up Table look-up Table create Table fold Table look-up		BCD number to its seven-				
codes of digit to be displayed are stored sequentially in memory. Table assign Table create Table fold Table look-up Table look-up Table create Table fold Table look-up Table look-up Table create Table fold Table look-up	150	segment code.	Convert	Ordered	Arrange	Delete
are stored sequentially in memory. Table assign Table create Table fold Table look-up Table look-up Table create Table fold Table look-up Table look-up Table create Table fold Table look-up Table look-up Table look-up Table look-up Table create Table fold Table look-up		In the technique, the				
Table assign Table create Table fold Table look-up The conversion program located the code of a digit based on its magnitude and transfer the code to the MPU to send out The American standard code for is used community in data community in data information intrachange interchange interchange interchange ASCII is a code. Table create Table fold Table look-up Table create Table fold Table look-up Table look-up Table create Table fold Table look-up Table look-up Input port display port HDD RAM ASCII is a code.		codes of digit to be displayed				
The conversion program located the code of a digit based on its magnitude and transfer the code to the MPU to send out 152		are stored sequentially in				
located the code of a digit based on its magnitude and transfer the code to the MPU to send out 152 to a Input port display port HDD RAM The American standard code for is used community in data information information information information intrachange interchange interchange 154 ASCII is a code. seven-bit six-bit five-bit four-bit	151	memory.	Table assign	Table create	Table fold	Table look-up
located the code of a digit based on its magnitude and transfer the code to the MPU to send out 152 to a Input port display port HDD RAM The American standard code for is used community in data information information information information intrachange interchange interchange 154 ASCII is a code. seven-bit six-bit five-bit four-bit		The conversion program				
the code to the MPU to send out to a Input port display port HDD RAM The American standard code for is used community in data information information information communication. intrachange interchange interchange ASCII is a code. seven-bit six-bit five-bit four-bit		located the code of a digit based				
152 to a Input port display port HDD RAM The American standard code for is used community in data community in data communication. information information information intercharge information intercharge intercharge 153 ASCII is a code. seven-bit six-bit five-bit four-bit		on its magnitude and transfer				
The American standard code for is used community in data information information information information intrachange interchange int		the code to the MPU to send out				
for is used community in data information information information intrachange interchange interchange interchange interchange intrachange interchange interc	152		Input port	display port	HDD	RAM
community in data information information information information intrachange interchange						
153communication.intrachangeinterchargeinterchangeinterchange154ASCII is a code.seven-bitsix-bitfive-bitfour-bit						
154 ASCII is a code. seven-bit six-bit five-bit four-bit		•				
	153	communication.	intrachange	intercharge	interchange	intracharge
	154	ASCII is a code.	seven-bit	six-bit	five-bit	four-bit
The hexadecimal number		The hexadecimal number				
represent 0 to 9 ASCII		represent 0 to 9 ASCII				
155 decimal number. 30H to 39H 0H to 9H 10H to 19H 20H to 29H	155		30H to 39H	0H to 9H	10H to 19H	20H to 29H
The hexadecimal number		The hexadecimal number				
represent capital letter						
156 A through Z ASCII. 41H to 5AH 00H to 26H 10H to 36H 20H to 46H	156		41H to 5AH	00H to 26H	10H to 36H	20H to 46H
When an ASCII character is]
entered the microprocessor		•				
receive the of ASCII decimal octal binary hexadecimal					•	
157 Hexa-decimal number. equivalent equivalent equivalent equivalent	157	Hexa-decimal number.	equivalent	equivalent	equivalent	equivalent

	When ASCII Key for digit 9 is				
	pressed the Microprocessor				
	receive the binary equivalent of				
	which must be				
	converted to the binary 1001 for				
158	arithmetic operation.	39H	29H	09H	19H
	When subtracting two BCD				
	number the instruction				
	cannot be used to decimal				
	adjust the result of two packed				
159	BCD number.	DAA	PCHL	ADD	ANA
	The of subtracted				
	can be added to illustrated 82 –		10's	20's	100's
160	48 = 34 can be performed.	1's complement	complement	complement	complement
	Multiplication can be			•	•
	performed by a this				
	technique is used in BCD -to-	repeated	repeated	repeated	repeated
161	binary conversion.	increment	addition	decrement	subtraction
	A is simply a				
	computer that enable the use of	software		hardware	
	modify, debug and text	development	software design	development	hardware
162	program.	system	system	system	design system
	includes program		,	· · · · · · · · · · · · · · · · · · ·	<i>U</i> ,
	that enable the user to develop				
	software in either assembly		hardware	software	
	language or high-level	software design	development	development	hardware
163	language.	system	system	system	design system
	Programs are accessed and		,	· · · · · · · · · · · · · · · · · · ·	- U
164	stored under	tag name	file name	folder name	object name
	is an optical disk that				3
	uses a laser beam to store				
	digital information on that can				
165	be read with a laser diode.	HDD	SSD	CDROM	RAM
	The kernel is a major			user	operating
166	component of an	software	circuit	application	system
	The is a program that			**	
	translate assembly language				
	memories or source code into				
167	binary executable code.	Assembler	Compiler	Linker	Loader
	In translation	-	1		
	requires that the source				
	program be written strictly				
	according to specified of				
168	assemble.	Assembler	Compiler	Linker	Loader
	8085 mnemonics are translated		r ·	-	hexadecimal
169	into	binary code	decimal code	octal code	code
	In assembler editor it is	<u>,</u>			
	instruction in				
	program quickly with new				
	memory location and modified	easy to insert or	difficult to	cannot insert	impossible to
170	address jump location.	delete	insert or delete	or delete	insert or delete
	The can reserve			2.2.22	
	memory location on for data				
171	result.	Compiler	Linker	Assembler	Loader
					

1 1	The 8085 has Vectored				
172	Interrupt	Five	Four	Three	Two
	is a Non Maskable				
173	interrupt.	RST 7.5	RST 6.5	TRAP	RST 5.5
	has the highest				
	priority among the interrupt				
174	signals.	RST 7.5	RST 6.5	TRAP	RST 5.5
	Theis a process of communication or data				
	transfer controlled by external				
175	peripheral.	DMA	CMA	CMP	DAA
173	реприста.	Divir	An interrupt	CIVII	Ditti
			that can be		
		An interrupt	turned off by	An interrupt	An interrupt
	What is meant by Maskable	which can never	the	that need	which has 3
176	interrupts?	be turned off.	programmer.	coding	pins
	After the completion of the				
1.77	DMA transfer, the processor is	Acknowledge	T	WANTED: 1	1101 D : 1
177	notified by	signal	Interrupt signal Three binary	WMFC signal Four binary	HOLD signal
178	Binary coded decimal is a combination of	Two binary digits	digits	digits	Five binary digits
170	The decimal number 90 is	digits	uigits	uigits	uigits
	represented in its BCD form as				
179	represented in its 2 c2 form ds	10100000	11010111	10010000	10101011
	Write the decimal equivalent				
180	for (00110001)BCD.	31	13	C1	1C
	Write the decimal equivalent				
181	for (00010011)BCD.	31	13	C1	1C
102	Invalid BCD can be converted	A 111	A 11:	C-1.4	C-1.4 4
182	to valid BCD by	Adding 6	Adding 66	Subtracting 6	Subtracting 66
183	Address line for RST 5.5 is?	'0020H	'0034H	'0028H	'002CH
184	Address line for RST 6.5 is?	'0020H	'0034H	'0028H	'002CH
185	Address line for RST 7.5 is?	'0020H	'003CH	'0028H	'002CH
186	Address line for TRAP is?	'0024H	'0034Н	'0028H	'002CH
	A is a sealed casing				
	aluminium box with a storage				
187	device that store digital data based on magnetic properties.	hard disk	SSD	CDROM	RAM
10/	A is a data storage	naru uisk	שמט	CDKOW	IXAIVI
	device that uses integrated				
	memory assemblies to store				
188	digital data.	hard disk	SSD	CDROM	RAM
	is a valid assembler				
189	directive.	END	ENX	EAX	DAX
100	is a valid assembler	FD. ***	T7 / **	5	07.5
190	directive.	ENX	EAX	DAX	ORG
191	is a valid assembler directive.	DW	EW	FW	MXX
191	is a valid assembler	DW	EW	L VV	MW
192	directive.	EQU	MQU	LQU	SQU
193	pin is Interrupt Read.	INTR	INTA	INR	DCR
193	pin is Interrupt Read.	IIVIK	INIA	IIVIX	DCK
194	Acknowledge.	INTR	INTA	INR	DCR
/					

	If interrupt is enabled and is high then 8085 accept				
195	interrupt.	INTR	INTA	INR	DCR
196	is a DMA signal.	HOLD	HLD	SHLD	LHLD
197	is a DMA signal.	HLDA	HLD	SHLD	LHLD
197	What is meant by Non-	An interrupt which can never	An interrupt that can be turned off by the	An interrupt that need	An interrupt which has 3
198	Maskable interrupts?	be turned off.	programmer.	coding	pins
	is a valid Maskable		1 0	<u> </u>	•
199	interrupt.	RST 8.5	RST 6.5	TRAP	RST 4.5
	is a valid Maskable				
200	interrupt.	RST 8.5	RST 7.5	TRAP	RST 4.5
201	Pentium select page table transition of linear address into address when PG=1.	Logical	physical	hardware	circuit
201	register is use to disable	Logicai	physical	naraware	Circuit
202	cache control of internal cache.	CD	AM	NP	TS
	register is use for			- ,-	
	alignment mask checking when				
203	set.	CD	WP	AM	TS
	register write protect user level page against supervision level write				
204	operation.	CD	AM	TS	WP
	register Indicates that				
205	the 80386 has switches task.	CD	AM	WP	TS
	is the process of		_		
206	controlling and coordinating	Memory	Process	File	Input output
206	computer memory.	management	management	management	management
207	stamp counter.	RDMSR	RDTSC	WRMSR	RSM
207	command read model	KDMSK	KDISC	WKWISK	KSWI
208	specific register.	RDMSR	RDTSC	WRMSR	RSM
	command write				
209	model specific register.	WRMSR	RDMSR	RDTSC	RSM
	command return from				
210	system management interrupt.	RSM	RDMSR	RDTSC	WRMSR
	The CMPXCHG				
	instruction is an extension of				
211	the CMPXCHG instruction	οn	9 <i>C</i>	0 1	6D
211	added to the 80486 instruction. The instruction reads	8B	8C	8A	8D
	the cup identification code and				
	other information from				
212	Pentium.	CPUID	CPUREAD	READCPU	IDCPU
	The version Information return				
	after executing the				
	Instruction with a logic 0 in				
213	EAX is returned in EAX.	CPUREAD	READCPU	IDCPU	CPUID
	In CPU version command, the				
214	family ID is returned in bit	0 to 2	1 +0 7	0 40 11	12 to 16
214	·	0 to 3	4 to 7	8 to 11	12 to 16

In CPU version command, the Stepping ID is returned in bit		In CPU version command, the				
In CPU version command, the Stepping ID is returned in bit 0 to 3	215	model ID is returned in bit	0 2	4 . 7	0 . 11	10 . 16
Stepping ID is returned in bit	215		0 to 3	4 to 7	8 to 11	12 to 16
For the Pentium II, the model number is and family		•				
For the Pentium II, the model number is and family ID is 3.	216	Stepping ID is returned in bit	O to 3	1 to 7	8 to 11	12 to 16
number is and family	210	For the Pentium II, the model	0 10 3	4107	0 10 11	12 to 10
The Memory Interface to the Pentium typically used the intel 218		· · · · · · · · · · · · · · · · · · ·				
The Memory Interface to the Pentium typically used the intel chipset. 700 600 850 900	217		4	5	6	7
Pentium typically used the intel chipset. Chipset.			·		-	,
Hyper threading is intel's technology for creating						
technology for creating	218	· - ·	700	600	850	900
Two Three Four		Hyper threading is intel's				
Any CPU that has a model ending with a means that the CPU is unlocked. This means that you can use setting to setup the clock speed of the chip. SUN SPARC is an instruction set Architecture IAS with integer and 32,64 and 128 bit 16 bit 32 bit 64 bit 128 bit		technology for creating				
Any CPU that has a model ending with a		logical core in each physical				
ending with ameans that the CPU is unlocked. This means that you can use setting to setup the clock speed of the chip.	219		One	Two	Three	Four
the CPU is unlocked. This means that you can use setting to setup the clock speed of the chip. 200		•				
means that you can use setting to setup the clock speed of the chip.						
The SPARC architecture recognizes fundamental 225 226 227 226 227 227 227 228 228 229 228 228 228 229 228 238 238 248 238 248 248 238 248 2						
SUN SPARC is an instruction set Architecture IAS with integer and 32,64 and 16 bit 32 bit 64 bit 128 bit						
SUN SPARC is an instruction set Architecture IAS with integer and 32,64 and 128 bit.	220		17	т		NT
Set Architecture IAS with integer and 32,64 and 128 bit.	220	•	K	L	M	N
integer and 32,64 and 16 bit 32 bit 64 bit 128 bit						
221 128 bit. 16 bit 32 bit 64 bit 128 bit						
SUN SPARC define general purpose integer floating point special status register and basics instructions operation. 32 16 72 80	221	-	16 hit	32 hit	6/1 hit	128 bit
Durpose integer floating point special status register and basics instructions operation. 32	221		10 010	32 OIt	04 010	120 011
Special status register and basics instructions operation. 32		•				
Description Supervisor mode User mode Admin mode Guest mode						
In the processor can execute any instruction including the privileged instruction.	222		32	16	72	80
execute any instruction including the privileged instruction. Supervisor mode User mode Admin mode Guest mode						
223						
Inan attempt to execute to execute privileges instruction will cause a trap to Supervisor Supervisor mode User mode Admin mode Guest mode		including the privileged				
to execute privileges instruction will cause a trap to Supervisor Software. Software. Supervisor mode User mode Admin mode Guest mode The SPARC architecture recognizes fundamental data formats (type) In SUN SPARC Signed integer can be bits. In SUN SPARC Unsigned integer can be bits. In SUN SPARC Floating-point can be bits. In SUN SPARC Floating-point can be bits. In SUN SPARC Halfword is bits. In SUN SPARC Halfword is bits. In SUN SPARC word size is bits. In SUN SPARC Tagged word is bits.	223		Supervisor mode	User mode	Admin mode	Guest mode
224 will cause a trap to Supervisor Supervisor mode User mode Admin mode Guest mode 224 Software. Supervisor mode User mode Admin mode Guest mode 225 The SPARC architecture recognizes fundamental data formats (type) One Two Three Four 226 In SUN SPARC Signed integer can be bits. 8, 16, 32 and 64 128 32, 64 and 128 64,128 and 256 227 In SUN SPARC Unsigned integer can be bits. 8, 16, 32 and 64 128 32, 64 and 128 64,128 and 256 228 In SUN SPARC Floating-point can be bits. 8, 16, 32 and 64 32, 64 and 128 64,128 and 256 229 bits. 16 32 64 128 229 bits. 16 32 64 128 230 bits. 16 32 64 128 230 bits. 16 32 64 128 231 is bits. 16(14+2) 32(30+2) 64(62+2) 128(126+2)		Inan attempt to execute				
224 Software. Supervisor mode User mode Admin mode Guest mode The SPARC architecture recognizes fundamental data formats (type) One Two Three Four 225 In SUN SPARC Signed integer can be bits. 8, 16, 32 and 64 128 32, 64 and 128 64,128 and 256 227 In SUN SPARC Unsigned integer can be bits. 8, 16, 32 and 64 128 32, 64 and 128 64,128 and 256 In SUN SPARC Floating-point can be bits. 8, 16, 32 and 64 32, 64 and 128 128 64,128 and 256 In SUN SPARC Halfword is In SUN SPARC Word size is bits. 16 32 64 128 230 bits. 16 32 64 128 In SUN SPARC Tagged word is bits. 16 32 64 128 231 is bits. 16(14+2) 32(30+2) 64(62+2) 128(126+2)		1 0				
The SPARC architecture recognizes fundamental data formats (type)	22.4					
225 recognizes fundamental data formats (type) One Two Three Four 226 In SUN SPARC Signed integer can be bits. 8, 16, 32 and 64 128 32, 64 and 128 64,128 and 256 In SUN SPARC Unsigned integer can be bits. 8, 16, 32 and 64 128 32, 64 and 128 64,128 and 256 In SUN SPARC Floating-point can be bits. 8, 16, 32 and 64 128 16, 32, 64 and 128 64,128 and 256 In SUN SPARC Halfword is 229 bits. 16 32 64 128 In SUN SPARC word size is 230 bits. 16 32 64 128 In SUN SPARC Tagged word 1s is bits. 16(14+2) 32(30+2) 64(62+2) 128(126+2)	224		Supervisor mode	User mode	Admin mode	Guest mode
225 data formats (type) One Two Three Four 226 In SUN SPARC Signed integer can be bits. 8, 16, 32 and 64 128 32, 64 and 128 64,128 and 256 In SUN SPARC Unsigned integer can be bits. 8, 16, 32 and 64 128 32, 64 and 128 64,128 and 256 In SUN SPARC Floating-point can be bits. 8, 16, 32 and 64 32, 64 and 128 128 64,128 and 256 In SUN SPARC Halfword is 229 bits. 16 32 64 128 In SUN SPARC word size is bits. 16 32 64 128 In SUN SPARC Tagged word is bits. 16 32 64 128 231 is bits. 16(14+2) 32(30+2) 64(62+2) 128(126+2)						
In SUN SPARC Signed integer 226 can be bits. 8, 16, 32 and 64 128 32, 64 and 128 64,128 and 256 In SUN SPARC Unsigned integer can be bits. 8, 16, 32 and 64 128 32, 64 and 128 64,128 and 256 In SUN SPARC Floating-point can be bits. 8, 16, 32 and 64 128 32, 64 and 128 64,128 and 256 In SUN SPARC Halfword is bits. 16 32 64 128 In SUN SPARC word size is bits. 16 32 64 128 In SUN SPARC Tagged word 16, 32 64 128 In SUN SPARC Tagged word 16 32 64 128 In SUN SPARC Tagged word 16 32 64 128 In SUN SPARC Tagged word 16 32 64 128 In SUN SPARC Tagged word 16 32 64 128 In SUN SPARC Tagged word 16 32 64 128 In SUN SPARC Tagged word 16 32 64 128 In SUN SPARC Tagged word 16 32 64 128 In SUN SPARC Tagged word 16 32 64 128 In SUN SPARC Tagged word 16 32 64 128 In SUN SPARC Tagged word 16 32 64 128 In SUN SPARC Tagged word 16 32 64 128 In SUN SPARC Tagged word 16 32 64 128 In SUN SPARC Tagged word 16 32 64 64 62 In SUN SPARC Tagged word 16 32 64 64 In SUN SPARC Tagged word 16 32 In SUN SPARC Tagged word 16 In SUN SPARC Tagged word 16 32 I	225	•	0	Т	Thus	Form
226 can be bits. 8, 16, 32 and 64 128 32, 64 and 128 64,128 and 256 In SUN SPARC Unsigned integer can be bits. 8, 16, 32 and 64 128 32, 64 and 128 64,128 and 256 In SUN SPARC Floating-point can be bits. 8, 16, 32 and 64 32, 64 and 128 128 64,128 and 256 In SUN SPARC Halfword is 229 bits. 16 32 64 128 In SUN SPARC word size is 230 bits. 16 32 64 128 In SUN SPARC Tagged word is bits. 16 32 64 128 In SUN SPARC Tagged word is bits. 16(14+2) 32(30+2) 64(62+2) 128(126+2)	223		One		Three	Four
In SUN SPARC Unsigned integer can be bits. 8, 16, 32 and 64 16, 32, 64 and 128 32, 64 and 128 64,128 and 256 In SUN SPARC Floating-point 228 In SUN SPARC Halfword is 229 16, 32, 64 and 128 128 64,128 and 256 In SUN SPARC Halfword is 230 16 32 64 128 In SUN SPARC word size is 230 16 32 64 128 In SUN SPARC Tagged word is bits. 16 32 64 128 In SUN SPARC Tagged word is bits. 16(14+2) 32(30+2) 64(62+2) 128(126+2)	226		8 16 32 and 64	· · · · ·	32 64 and 128	64 128 and 256
227 integer can be bits. 8, 16, 32 and 64 128 32, 64 and 128 64,128 and 256 In SUN SPARC Floating-point can be bits. 8, 16, 32 and 64 32, 64 and 128 128 64,128 and 256 In SUN SPARC Halfword is 229 bits. 16 32 64 128 In SUN SPARC word size is 230 bits. 16 32 64 128 In SUN SPARC Tagged word is bits. 16 32 64 128 231 is bits. 16(14+2) 32(30+2) 64(62+2) 128(126+2)	220		5, 10, 52 and 04		52, 07 and 120	07,120 and 230
228 In SUN SPARC Floating-point can be bits. 8, 16, 32 and 64 32, 64 and 128 16, 32, 64 and 128 64,128 and 256 In SUN SPARC Halfword is 16 32 64 128 In SUN SPARC word size is 16 32 64 128 In SUN SPARC word size is 16 32 64 128 In SUN SPARC Tagged word 16 32 64 128 231 is bits. 16(14+2) 32(30+2) 64(62+2) 128(126+2)	2.2.7	•	8, 16, 32 and 64		32, 64 and 128	64.128 and 256
228 can be bits. 8, 16, 32 and 64 32, 64 and 128 128 64,128 and 256 In SUN SPARC Halfword is 16 32 64 128 In SUN SPARC word size is 230 bits. 16 32 64 128 In SUN SPARC Tagged word 16 32 64 128 231 is bits. 16(14+2) 32(30+2) 64(62+2) 128(126+2)			5, 15, 52 and 54	120	·	5 1,120 and 250
229 bits. 16 32 64 128 In SUN SPARC word size is 230 bits. 16 32 64 128 In SUN SPARC Tagged word 16 32 64 128 231 is bits. 16(14+2) 32(30+2) 64(62+2) 128(126+2)	228	9	8, 16, 32 and 64	32, 64 and 128		64,128 and 256
229 bits. 16 32 64 128 In SUN SPARC word size is bits. 16 32 64 128 In SUN SPARC Tagged word bits. 16(14+2) 32(30+2) 64(62+2) 128(126+2)			, , ,	,	-	,
In SUN SPARC word size is	229		16	32	64	128
In SUN SPARC Tagged word 231 is bits.						
231 is bits. 16(14+2) 32(30+2) 64(62+2) 128(126+2)	230	bits.	16	32	64	128
		In SUN SPARC Tagged word				
232 In SUN SPARC Double word is 16 32 64 128	231	is bits.	16(14+2)	32(30+2)	64(62+2)	128(126+2)
i l l	232	In SUN SPARC Double word is	16	32	64	128

	bits.				
	In SUN SPARC Quad word is				
233	bits.	16	32	64	128
	In SUN SPARC,				
	instruction are the only				
234	instruction that access memory.	load/store	immediate	Arithmetic	Branching
	In SUN SPARC, the read/write				
	register instruction read and				
	write the content of		hardware		
235	state / status register.	software visible	visible	logical visible	machine visible
	The address bus on the Pentium				
	pro the widened to 36 bit,				
	giving it maximum address bit				
236	of GB memory.	64	32	16	128
	In Pentium pro instruction				
	flowing down the execution can			sequentially	
237	complete	never	easier	only	out of order
	The Pentium pro is optimized				
	for numbing a bit				
238	application code.	16	32	64	128
	The Pentium pro dramatically,				
	increases the number of				
	execution step to from				
239	Pentium.	12	14	16	32
	The Pentium pro achieve				
	performance approximately.				
240	% higher than a Pentium	25	70	7.5	100
240	of some clock speed.	25	50	75	100
241	Pentium pro have integrated level cache.	1	2	3	4
241		1	<u> </u>	3	4
	The memory management unit within the Pentium is upward				
	compatible with the				
242	microprocessor.	80386	80186	80185	80154
272	The Pentium paging mechanism	00300	00100	00103	00154
	function with memory				
243	page.	2k- byte	4k- byte	8k- byte	16k- byte
	The new Pentium new			011 0 9 00	
	extension uses page size of				
244	bytes.	1M	2M	4M	8M
	The interrupt disable all				
	other interrupt that are normally				
	handled by user application and				
245	operating system.	SMI	IMS	IMMS	IMS
	EAX register is bit				
246	register.	8	16	32	64
	The Pentium 4 was released in				
247		36831	37196	40483	44136
	The Pentium 4(Nov 2000) has				
248	clock speed of	1.3Ghz	600Mhz	1.8Ghz	2.5Ghz
	The Pentium 4 uses				
	micron technology for				
249	fabrication.	18	180	1.8	0.18
250	A dual core processor has	1	2	3	4

		_	_
internal processor.			