PUNE VIDYARTHI GRIHA'S

COLLEGE OF SCIENCE AND TECHNOLOGY

Affiliated to University of Mumbai

Question Bank

Class: F.Y.B. Sc.IT **Semester: II**

Subject: Microprocessor Architecture

Sr no	Question	A	B	C	D
1	Microprocessor was introduced in the year _____.	1945	1971	1974	1980
2	Flip – flops are used in a microprocessor to indicate _____.	Shift register	latches	counters	flags
3	The number of address lines required to access 64 Kbyte of memory of the microprocessor is _____.	16	32	20	8
4	Flip –flops are used in a microprocessor to indicate _____.	shift register	latch	counters	flag
5	The first microprocessor was _____.	4001	8085	4003	4004
6	Which of the following microprocessor has an 8 bit data bus _____.	4004	80186	8085	8086
7	The number of flags in 8085 are _____.	4	8	6	5
8	A microprocessor is _____.	an analog device	a digital device	an analog and digital device	hybrid device
9	The 16 bit processor is _____.	8085	8086	80486	pentium
10	The data bus of microprocessor is _____.	unidirectional	bi –directional	unidirectional as well as bi directional	semi - directional
11	Which system communicates with the outside word via the I/O devices interfaced to it:	Microprocessor	Microcomputer	Digital computer	Hybrid computer
12	How many generation of microprocessor?	Four	Five	Six	Three
13	Each machine cycle consists of many clock periods called as_____.	t-states	instruction cycle	fetch cycle	machine cycle
14	The length of LXI H, 9000H is _____ .	one-byte	two-byte	three-byte	four-byte

15	Why 8085 processor is called an 8 bit processor?	because 8085 processor has 8 bit ALU	because 8085 processor has 8 bit data bus	because 8085 processor has 16 bit data bus	because 8085 processor has 16 bit address bus
16	The address / data bus in 8085 is _____.	multiplexed	demultiplexed	decoded	encoded
17	In 8085 name the 16 bit registers?	Accumulator	Program counter	Instruction decoder	ALU
18	____ pin of 8085 is useful for interfacing low speed devices.	Ready	RIM	ALE	SIM
19	Machine language instruction format consist of _____.	Operation code field	Operation code field & operand field	Operand field	none of the mentioned
20	Assembly language programs are written using _____.	Hex code	Mnenonics	ASCII code	None of these View
21	How many types of Interfacing does a microprocessor have?	2	3	4	5
22	Which of the following are known as Higher Address Bus?	A15 - A8	AD7 - AD0	READY	WR
23	DMA stands for?	Display Memory Access	Directly Memory Access	Device Memory Access	Direct Memory Access
24	Which of the following is not true features of 8257?	It has three channels which can be used over three I/O devices.	Each channel has 16-bit address and 14-bit counter.	Each channel can transfer data up to 64kb.	Each channel can be programmed independently.
25	A microprocessor instruction set can be classified into?	2	3	4	5
26	Microprocessor 8085 is a _____ bit processor.	4	8	16	32
27	There are _____ address lines in Microprocessor 8085.	4	8	16	32
28	The data bus consists of _____ lines.	4	8	16	32
29	_____ bus is bi-directional.	Data	Address	Control	Memory
30	_____ Register is part of ALU.	A	B	C	D
31	Register A is of _____ bits in Microprocessor 8085.	4	8	16	32
32	Each instruction has two parts: one is task to be performed, called the _____.	opcode	operand	Instruction	mnenonics
33	Each instruction has two parts: one is data to be operated on called the _____.	opcode	operand	Instruction	mnenonics
34	A _____ instruction includes the op-code and operand in the same byte.	one-byte	two-byte	three-byte	four-byte
35	In a three-byte instruction, the first byte specifies the _____.	opcode	operand	Instruction	mnenonics
36	In a three-byte instruction, the	opcode	lower order	lower order	higher order

	second byte specifies the _____.		address	address or data	address
37	In a three-byte instruction, the third byte specifies the _____.	opcode	lower order address	higher order address or data	higher order address
38	In a two-byte instruction, the second byte specifies the _____.	opcode	operand	Instruction	mnenonics
39	_____ is defined as the time interval between 2-trailing or leading edges of the clock.	t-states	instruction cycle	fetch cycle	machine cycle
40	The total time required to execute an instruction given by _____.	IC = Fc - Ec	IC = Fc + Ec	IC = Fc + Mc	IC = Mc + Ec
41	Low level computer language are also called as _____.	Assembly language	Programming language	Machine language	mnenonics
42	Middle level computer language are also called as _____.	Assembly language	Programming language	Machine language	mnenonics
43	_____ are high-speed computers, and their word length generally ranges from 32 to 64 bit.	Large computer	Mainframe	Medium size	Microcomputer
44	_____ operation accepts data from input devices.	Memory Read	Memory Write	I/O read	I/O Write
45	_____ operation sends data to output devices.	Memory Read	Memory Write	I/O read	I/O Write
46	Microprocessor 8085 can operate on clock cycle with ____% duty cycle.	20	40	50	60
47	This is a +ve pulse generated every time when 8085 begins an operation(machine cycle); it indicates that the bits on AD0 – AD7 are address bits.	RD	WR	ALE	HOLD
48	When the signal on this pin goes low, the program counter is set to zero the buses are tri-stated and the MPU is Reset.	RD	RESET OUT	ALE	RESET IN
49	Having received _____ request the microprocessor relinquishes the use of the buses as soon as the current machine cycle is completed.	Ready	RESET OUT	ALE	RESET IN
50	The data on this line is loaded into accumulator whenever a RIM instruction is executed.	Ready	RIM	ALE	SIM
51	STA 4000 is_____byte instruction.	one	three	two	four
52	RAL is an example of _____ addressing mode.	register	direct	implied	immediate
53	Stack pointer is a -------- register.	16 bit	8 bit	32 bit	4bit
54	In memory mapped I/O device	8bit address	IN		OUT

	is identified by _____.		instruction16bit address		instruction
55	In I/O mapped input device is _____.	latch	buffer	decoder	stack
56	In I/O mapped output device is _____.	buffer	encoder	latch	stack
57	If accumulator content is 88H, after execution of CMA accumulator content will be _____.	77H	93H	FFH	80H
58	LDA is ---------Instruction.	arithmetic	logical	branch	data transfer
59	If A=56H,B=82H after execution of ANA B ,content of A= -----.	02H	56H	00H	D8H
60	8085 has EPROM of _____.	1Kb	526bytes	64kb	256 bytes
61	In 8085, 16-bit address bus, which can address upto?	16KB	32KB	64KB	128KB
62	There are _____ general purpose registers in 8085 processor.	5	6	7	8
63	It is also a 16-bit register works like stack, which is always incremented/decremented by 2 during push & pop operations.	Stack pointer	Temporary register	Flag register	Program counter
64	Flag register is an 8-bit register having _____ 1-bit flip-flops.	3	4	5	6
65	What is true about Program counter?	It is an 8-bit register, which holds the temporary data of arithmetic and logical operations.	When an instruction is fetched from memory then it is stored in the program counter	It provides timing and control signal to the microprocessor	It is a 16-bit register used to store the memory address location of the next instruction to be executed.
66	This signal indicates that another master is requesting the use of the address and data buses.	READY	HOLD	HLDA	INTA
67	This signal is used as the system clock for devices connected with the microprocessor.	X1, X2	CLK OUT	CLK IN	IO/M
68	Which of the following is true about Control and status signals?	These signals are used to identify the nature of operation.	There are 3 control signal and 3 status signals.	Three status signals are IO/M, S0 & S1.	All of the above
69	The register in the 8085A that is used to keep track of the memory address of the next op-code to be run in the program is the:	stack pointer	program counter	instruction pointer	accumulator
70	The data bus in 8080A/8085	eight	sixteen	eight	eight lines used

	microprocessor is a group of _____.	bidirectional lines that are used to transfer 8 bits between the microprocessor and its I/O and memory	bidirectional lines that are used for data transfer between the microprocessor and memory	unidirectional lines that are used for I/O devices	to transfer data among the registers
71	In 8085, to disable the whole interrupt system (except TRAP).	the DI instruction may be used	the DO instruction may be used	the INTERRUPT instruction may be used	the El instruction may be used
72	Exceptions to the 8085 microprocessor normal operation are called:	jump instructions	decoding	interrupts	jump instructions or interrupts
73	In 8085 microprocessor, which of the following interrupts has the highest priority?	RST 5.5	RST 7.5	TRAP	INTR
74	Which of the following was not a design improvement for the 8086/8088 over the 8085?	Execution unit (EU)	16-bit data bus	Arithmetic logic unit (ALU)	Bus interface unit (BIU)
75	How many buses are connected as part of the 8085A microprocessor?	2	3	5	6
76	Register A is of _____ bits in Microprocessor 8085.	4	8	16	32
77	All the arithmetic and logic operations are done considering _____ as one of the operand register.	A	B	C	D
78	Program counter register of Microprocessor 8085 is of _____ bits.	4	8	16	32
79	One of the following register is of 16-bits.	D	E	F	SP
80	One of the following is not a Register of Microprocessor 8085.	E	C	L	F
81	_____ instruction transfers the contents from Reg A to Reg B.	MOV A,B	MOV B,A	ADI B	ADI A
82	Register _____ is a part of ALU.	A	B	C	D
83	After any arithmetic or logic operation the result is generally stored in Register.	H	L	F	A
84	The instruction for comparing the contents of register is.	CMA	CMP	CPM	CPI
85	There are _____ Rotate instructions in 8085.	2	3	4	5
86	The rotate instruction rotates the contents of _____ Register.	A	B	C	D
87	One of the following is an invalid register pair.	AB	BC	DE	HL
88	To address a memory chip	8	9	10	11

	having 1024 registers _____ address lines are used.				
89	The total memory capacity of 8085 is ____ bytes.	32K	64K	128K	512K
90	For a microprocessor based system the system performance is given by.	Address Bus	Data Bus	Control Bus	All Bus
91	For a microprocessor based system the system capacity is given by _____.	Address Bus	Data Bus	Control Bus	All Bus
92	The instruction _____ adds the contents of Reg A with Reg C in 8085.	ADD A	ADD C	ADD C,A	ADDA,C
93	The memory location in MOV A,M is pointed by _____ register pair.	BC	DE	HL	BE
94	One of the following is an invalid instruction of 8085.	STAX A	LDAX B	STAX D	LDAX D
95	One of the following is not a valid register pair in 8085 _____.	AB	BC	DE	HL
96	The instruction LXI H, 1020 is a _____ byte instruction.	1	2	3	4
97	One of the following is 2 byte instruction _____.	ADI 12	LDAX B	STAX D	MOV M,A
98	One of the following is a logic instruction _____.	ADD A	ANA B	SUB C	DCR C
99	There are _____ conditional jumps in 8085 _____.	4	6	7	8
100	One of the following represents an umconditional jump in 8085 _____.	JNC	JZ	JM	JMP
101	In which of these modes, the immediate operand is included in the instruction itself?	register operand mode	immediate operand mode	register and immediate operand mode	none of the mentioned
102	A sequence of two registers that multiplies the content of DE register pair by two and stores the result in HL register pair (in 8085 assembly language) is _____.	XCHG & DAD B	XTHL & DAD H	PCHL & DAD D	XCHG & DAD H
103	The accumulator contains 85H, register B contains 68H, what is the content of accumulator and CY (carry) after executing the following code? ADD B DAA	35H, 1	53H, 0	35H, 0	53H, 1
104	Which instruction is required to rotate the content of accumulator one bit right along with carry?	RLC	RAL	RRC	RAR
105	The accumulator contains 03H	83H, 0	38H, 0	83H, 1	38H, 1

	and register D containd 81H, what is the content of the accumulator and the CY after executing ORA D?				
106	Register pair used to indicate memory _____.	B and C	D and E	H and L	W and Z
107	What are software interrupts?	RST 0-7	RST 5.5 - 7.5	INTR, TRAP	RST 4.4 - 6.4
108	For one's complement following instruction is use.	CMA	CMP	CMC	CMT
109	For Exchanging data following instruction is used.	Exchange	XCHG	Change	EXCH
110	Checking for errors in the program by observing the execution of instruction is _____.	Static debugging	Reg debugging	Dynamic debugging	A & C
111	The time required for the execution of the program depends on ____.	t-states	instruction cycle	fetch cycle	machine cycle
112	_____ instruction use to adjust result to BCD.	DAD	DDA	DAA	ADA
113	CMA ADI 01H above code will perform .	calculate 1's complement	calculate 2's complement	addition	complement
114	DAD B means _____.	HL+BC	H+B	L+C	D+B
115	SBB B instruction says _____.	A-B-Borrow	B-B	B-B-Borrow	A & B
116	The accumulator contains 77H and register D containd 56H, what is the Content of the accumulator and the CY after executing XRA D?	21H, 1	12H, 0	21H, 0	12H, 1
117	To generate a delay using 8 bit counter _____.	MVI D, Count L1: DCR D JNZ L1	MOV D, Count L1: DCR D JNZ L1	MVI D, Count L1: DCX D JNZ L1	MOV D, Count L1: DCX D JNZ L1
118	What is the length of the temporary register of 8085 microprocessor?	32 bits	12 bits	16 bits	8 bits
119	How many I/O ports can be accessed by direct method in 8085 microprocessor?	8	128	256	64
120	What is the addressing mode used in instruction MOVE M, C ?	Direct	Induced	Indirect	Immediate
121	What addressing mode is used in the instruction LDA 0345H ?	Direct	Implied	Indirect	Immediate
122	The accumulator contains 39H, register C contains 12H, what is the content of accumulator and CY (carry) after executing the following code?	05H, 1	50H, 1	51H, 0	50H,0
123	Two 8-bit temporary registers of 8085 microprocessor?	B & C	D & E	W & Z	H & L
124	Registers exclusively used for the internal operation by the	B & C	D & E	W & Z	H & L

	microprocessor _____.				
125	This instruction copies H and L register to the stack pointer _____.	SPHL	XTHL	CPHL	HLSP
126	This instruction exchanges H and L with top of stack _____.	SPHL	XTHL	CPHL	HLSP
127	Outcome of OUT F8H _____.	Copy data from i/p to device with address F8	Copy data from Accumulator to o/p device with address F8	Copy F8 to Output port	Copy from i/p device with address F8 to Accumulator
128	ADD B is a _____ byte instruction.	1	2	3	4
129	LDA 2050H will _____.	Load contents of memory location 2050H into A	Load contents of I/O location 2050H into A	Load contents of A into memory location 2050H	Load contents of A into I/O location 2050H
130	JP stands for _____.	Jump on Parity	Jump on Plus	Jump on Positive	Jump on Prime
131	LDAX C _____.	is an incorrect instruction	copies data into Accumulator	Copies memory location	None of the above
132	A= AAH. CY = 0. On executing RLC. A will become ____.	45H	55H	BBH	AAH
133	DAA command stands for _____.	Divide Accumulator Arithmetic	Decimal Accumulator Arithmetic	Divide Adjust Accumulator	Decimal Adjust Accumulator
134	ANA B will _____.	Logical AND register B with the accumulator	Logical AND register B with B	Logical AND register B with i/p	Logical AND register B with o/p
135	ANI 01 will _____.	Logical AND immediate 01 with the accumulator	Logical AND immediate port address 01 with the accumulator	Logical AND immediate 01 with 01	Logical AND immediate accumulator with itself
136	XRA M will _____.	Exclusive OR memory with the accumulator	OR memory with the accumulator	Exclusive OR M register with the accumulator	OR M Register with the accumulator
137	Instruction RPE will _____.	Return from the subroutine if parity flag is 0	Return from the subroutine if parity flag is 1	Return from the subroutine if Positive	Return from the subroutine if Prime
138	Instruction RM will ____.	Returns from the subroutine if sign flag is 0	Returns from the subroutine if mean is 1	Returns from the subroutine if sign flag is 1	Returns from the subroutine if minus is 1
139	Push value of accumulator and flag in stack.	STACK FLAGS	PUSH FLAGS,A	PUSH A,FLAGS	PUSH PSW
140	POP H.	Pop value from TOP of memory stack in H	Pop value of H to Accumulator	Pop value from bottom of memory stack in H	Pop value memory in H

141	In the below code , how many times will DCR B Instruction get executed? MVI B,FFHLOOP: DCR B JNZ LOOP RET	256	255	128	512
142	JNZ LOOP will require how many t-states?	10	14	12	6
143	RAL instruction will _____.	Rotate accumulator left through carry	Rotate accumulator left without carry	Rotate all left through carry	Rotate all left without carry
144	SHLD us a _____ byte instruction.	1	2	3	4
145	SHLD instruction will _____.	Store HL registers Direct	Store HL registers Indirect	Store into HL registers Indirect	Store into HL registers Indirect
146	Copy H & L registers into Program counter.	HLPC	PCHL	CPHL	CPPC
147	STC will ____.	Set the Carry Flag	Subtract the Contents	Subtract the Carry	Set the Accumulator
148	XCHG will _____.	Exchange contents of HL & DE	Exchange contents of HL & PC	Exchange contents of BC & HL	Exchange contents of HL & SP
149	_____ is a valid Maskable interrupt.	RST 8.5	TRAP	RST 5.5	RST 4.5
150	When a BCD number is to be displayed by a seven-segment led, it is necessary to _____ the BCD number to its seven-segment code.	Convert	Ordered	Arrange	Delete
151	In the _____ technique, the codes of digit to be displayed are stored sequentially in memory.	Table assign	Table create	Table fold	Table look-up
152	The conversion program located the code of a digit based on its magnitude and transfer the code to the MPU to send out to a _____.	Input port	display port	HDD	RAM
153	The American standard code for _____ is used community in data communication.	information intrachange	information intercharge	information interchange	information intracharge
154	ASCII is a _____ code.	seven-bit	six-bit	five-bit	four-bit
155	The hexadecimal number _____ represent 0 to 9 ASCII decimal number.	30H to 39H	0H to 9H	10H to 19H	20H to 29H
156	The hexadecimal number _____ represent capital letter A through Z ASCII.	41H to 5AH	00H to 26H	10H to 36H	20H to 46H
157	When an ASCII character is entered the microprocessor receive the _____ of ASCII Hexa-decimal number.	decimal equivalent	octal equivalent	binary equivalent	hexadecimal equivalent

158	When ASCII Key for digit 9 is pressed the Microprocessor receive the binary equivalent of _____ which must be converted to the binary 1001 for arithmetic operation.	39H	29H	09H	19H
159	When subtracting two BCD number the instruction _____ cannot be used to decimal adjust the result of two packed BCD number.	DAA	PCHL	ADD	ANA
160	The _____ of subtracted can be added to illustrated 82 – 48 =34 can be performed.	1's complement	10's complement	20's complement	100's complement
161	Multiplication can be performed by a _____ this technique is used in BCD -to-binary conversion.	repeated increment	repeated addition	repeated decrement	repeated subtraction
162	A _____ is simply a computer that enable the use of modify, debug and text program.	software development system	software design system	hardware development system	hardware design system
163	_____ includes program that enable the user to develop software in either assembly language or high-level language.	software design system	hardware development system	software development system	hardware design system
164	Programs are accessed and stored under _____.	tag name	file name	folder name	object name
165	_____ is an optical disk that uses a laser beam to store digital information on that can be read with a laser diode.	HDD	SSD	CDROM	RAM
166	The kernel is a major component of an _____.	software	circuit	user application	operating system
167	The _____ is a program that translate assembly language memories or source code into binary executable code.	Assembler	Compiler	Linker	Loader
168	In _____ translation requires that the source program be written strictly according to specified of assemble.	Assembler	Compiler	Linker	Loader
169	8085 mnemonics are translated into _____.	binary code	decimal code	octal code	hexadecimal code
170	In assembler editor it is _____ instruction in program quickly with new memory location and modified address jump location.	easy to insert or delete	difficult to insert or delete	cannot insert or delete	impossible to insert or delete
171	The _____ can reserve memory location on for data result.	Compiler	Linker	Assembler	Loader

172	The 8085 has _____ Vectored Interrupt	Five	Four	Three	Two
173	_____ is a Non Maskable interrupt.	RST 7.5	RST 6.5	TRAP	RST 5.5
174	_____ has the highest priority among the interrupt signals.	RST 7.5	RST 6.5	TRAP	RST 5.5
175	The _____is a process of communication or data transfer controlled by external peripheral.	DMA	CMA	CMP	DAA
176	What is meant by Maskable interrupts?	An interrupt which can never be turned off.	An interrupt that can be turned off by the programmer.	An interrupt that need coding	An interrupt which has 3 pins
177	After the completion of the DMA transfer, the processor is notified by _____	Acknowledge signal	Interrupt signal	WMFC signal	HOLD signal
178	Binary coded decimal is a combination of _____	Two binary digits	Three binary digits	Four binary digits	Five binary digits
179	The decimal number 90 is represented in its BCD form as _____	10100000	11010111	10010000	10101011
180	Write the decimal equivalent for (00110001)BCD.	31	13	C1	1C
181	Write the decimal equivalent for (00010011)BCD.	31	13	C1	1C
182	Invalid BCD can be converted to valid BCD by ____.	Adding 6	Adding 66	Subtracting 6	Subtracting 66
183	Address line for RST 5.5 is?	‘0020H	‘0034H	‘0028H	‘002CH
184	Address line for RST 6.5 is?	‘0020H	‘0034H	‘0028H	‘002CH
185	Address line for RST 7.5 is?	‘0020H	‘003CH	‘0028H	‘002CH
186	Address line for TRAP is?	‘0024H	‘0034H	‘0028H	‘002CH
187	A _____ is a sealed casing aluminium box with a storage device that store digital data based on magnetic properties.	hard disk	SSD	CDROM	RAM
188	A _____ is a data storage device that uses integrated memory assemblies to store digital data.	hard disk	SSD	CDROM	RAM
189	_____is a valid assembler directive.	END	ENX	EAX	DAX
190	_____is a valid assembler directive.	ENX	EAX	DAX	ORG
191	_____is a valid assembler directive.	DW	EW	FW	MW
192	_____ is a valid assembler directive.	EQU	MQU	LQU	SQU
193	_____ pin is Interrupt Read.	INTR	INTA	INR	DCR
194	_____ pin is Interrupt Acknowledge.	INTR	INTA	INR	DCR

195	If interrupt is enabled and _____ is high then 8085 accept interrupt.	INTR	INTA	INR	DCR
196	_____ is a DMA signal.	HOLD	HLD	SHLD	LHLD
197	_____ is a DMA signal.	HLDA	HLD	SHLD	LHLD
198	What is meant by Non-Maskable interrupts?	An interrupt which can never be turned off.	An interrupt that can be turned off by the programmer.	An interrupt that need coding	An interrupt which has 3 pins
199	_____ is a valid Maskable interrupt.	RST 8.5	RST 6.5	TRAP	RST 4.5
200	_____ is a valid Maskable interrupt.	RST 8.5	RST 7.5	TRAP	RST 4.5
201	Pentium select page table transition of linear address into _____ address when PG=1.	Logical	physical	hardware	circuit
202	_____ register is use to disable cache control of internal cache.	CD	AM	NP	TS
203	_____ register is use for alignment mask checking when set.	CD	WP	AM	TS
204	_____ register write protect user level page against supervision level write operation.	CD	AM	TS	WP
205	_____ register Indicates that the 80386 has switches task.	CD	AM	WP	TS
206	_____ is the process of controlling and coordinating computer memory.	Memory management	Process management	File management	Input output management
207	_____ command return time stamp counter.	RDMSR	RDTSC	WRMSR	RSM
208	_____command read model specific register.	RDMSR	RDTSC	WRMSR	RSM
209	_____ command write model specific register.	WRMSR	RDMSR	RDTSC	RSM
210	_____ command return from system management interrupt.	RSM	RDMSR	RDTSC	WRMSR
211	The CMPXCHG _____ instruction is an extension of the CMPXCHG instruction added to the 80486 instruction.	8B	8C	8A	8D
212	The _____ instruction reads the cup identification code and other information from Pentium.	CPUID	CPUREAD	READCPU	IDCPU
213	The version Information return after executing the ____ Instruction with a logic 0 in EAX is returned in EAX.	CPUREAD	READCPU	IDCPU	CPUID
214	In CPU version command, the family ID is returned in bit _____.	0 to 3	4 to 7	8 to 11	12 to 16

215	In CPU version command, the model ID is returned in bit _____.	0 to 3	4 to 7	8 to 11	12 to 16
216	In CPU version command, the Stepping ID is returned in bit _____.	0 to 3	4 to 7	8 to 11	12 to 16
217	For the Pentium II, the model number is _____ and family ID is 3.	4	5	6	7
218	The Memory Interface to the Pentium typically used the intel _____ chipset.	700	600	850	900
219	Hyper threading is intel's technology for creating _____ logical core in each physical core.	One	Two	Three	Four
220	Any CPU that has a model ending with a _____ means that the CPU is unlocked. This means that you can use setting to setup the clock speed of the chip.	K	L	M	N
221	SUN SPARC is an instruction set Architecture IAS with _____ integer and 32,64 and 128 bit.	16 bit	32 bit	64 bit	128 bit
222	SUN SPARC define general purpose integer floating point special status register and ___ basics instructions operation.	32	16	72	80
223	In _____ the processor can execute any instruction including the privileged instruction.	Supervisor mode	User mode	Admin mode	Guest mode
224	In _____an attempt to execute to execute privileges instruction will cause a trap to Supervisor Software.	Supervisor mode	User mode	Admin mode	Guest mode
225	The SPARC architecture recognizes _____ fundamental data formats (type)	One	Two	Three	Four
226	In SUN SPARC Signed integer can be _____ bits.	8, 16, 32 and 64	16, 32, 64 and 128	32, 64 and 128	64,128 and 256
227	In SUN SPARC Unsigned integer can be _____ bits.	8, 16, 32 and 64	16, 32, 64 and 128	32, 64 and 128	64,128 and 256
228	In SUN SPARC Floating-point can be _____ bits.	8, 16, 32 and 64	32, 64 and 128	16, 32, 64 and 128	64,128 and 256
229	In SUN SPARC Halfword is _____ bits.	16	32	64	128
230	In SUN SPARC word size is ___ bits.	16	32	64	128
231	In SUN SPARC Tagged word is _____ bits.	16(14+2)	32(30+2)	64(62+2)	128(126+2)
232	In SUN SPARC Double word is	16	32	64	128

	_____ bits.				
233	In SUN SPARC Quad word is _____ bits.	16	32	64	128
234	In SUN SPARC, _____ instruction are the only instruction that access memory.	load/store	immediate	Arithmetic	Branching
235	In SUN SPARC, the read/write register instruction read and write the content of _____ state / status register.	software visible	hardware visible	logical visible	machine visible
236	The address bus on the Pentium pro the widened to 36 bit, giving it maximum address bit of _____ GB memory.	64	32	16	128
237	In Pentium pro instruction flowing down the execution can complete_____.	never	easier	sequentially only	out of order
238	The Pentium pro is optimized for numbing a _____ bit application code.	16	32	64	128
239	The Pentium pro dramatically, increases the number of execution step to _____ from Pentium.	12	14	16	32
240	The Pentium pro achieve performance approximately. _____% higher than a Pentium of some clock speed.	25	50	75	100
241	Pentium pro have integrated level _____ cache.	1	2	3	4
242	The memory management unit within the Pentium is upward compatible with the _____ microprocessor.	80386	80186	80185	80154
243	The Pentium paging mechanism function with _____ memory page.	2k- byte	4k- byte	8k- byte	16k- byte
244	The new Pentium new extension uses page size of ____ bytes.	1M	2M	4M	8M
245	The _____ interrupt disable all other interrupt that are normally handled by user application and operating system.	SMI	IMS	IMMS	IMS
246	EAX register is _____ bit register.	8	16	32	64
247	The Pentium 4 was released in _____.	36831	37196	40483	44136
248	The Pentium 4(Nov 2000) has clock speed of _____.	1.3Ghz	600Mhz	1.8Ghz	2.5Ghz
249	The Pentium 4 uses _____ micron technology for fabrication.	18	180	1.8	0.18
250	A dual core processor has	1	2	3	4

	_____ internal processor.				